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Modeling and Design of Cascaded h-bridge type multi-level Inverters up to Thirty-one level for the Reduction and Performance Improvement

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Abstract: ***Multilevel inverter (MLI) becomes more popular in high voltage DC (HVDC) applications, power electronic converters and drives. This paper describes the simulation of single phase multilevel cascaded H-bridge inverter. Simulation of three level, five level, thirteen level, fifteen, twenty-one, thirty-one level inverters are done in MATLAB/ Simulink. The switching schemes, and topologies are discussed in detail here up to thirty-one levels. This paper discusses the voltage level to achieve sinusoidal waveform & compare different voltage level by increasing the level through simulation. The closed loop space-vector based pulse width modulation technique is adopted for effective controlling and lower harmonic voltage conversion. The comparative results are presented for multilevel inverter up-to thirty-one level which shows the total harmonic distortion (THD) is decreased as the number of voltage level rises.***

Keywords: ***Multi-level Inverters, Sinusoidal pulse width modulation, cascaded H-bridge inverter, total harmonic distortion, selective harmonic reduction***

I. INTRODUCTION

The output voltage is obtained in various levels of steps so called as multi-level inverter (MLI). These MLI are used mainly in medium and high-power applications like motor drives, power electronic load control and high voltage applications [1]. These MLI will produce sinusoidal voltage in steps for levels starting from three level making it more sinusoidal than is produced with a general converter switches. Beyond this, the blocking voltage capability of two-level inverters is poor to handle medium voltage and power applications. Also, dv/dt rating is poor, total harmonic distortion (THD) is very high, meeting of modern grid codes during abnormal grid conditions is poor for the two-level conventional inverter. Also, stress on these switching devices is high, power dissipation is more and efficiency is lesser for two level inverters compared to higher level inverter and also results in higher electromagnetic and other interferences [2 and 3].

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There are three major classes of MLI, neutral-point based multi-level inverter, cascaded and flying capacitor kind and among cascaded H-bridge modular multi-level inverters are more prominent [4 and 5]. The modern-day application of MLI includes High-Voltage Direct-Current (HVDC) [6-7], motor drives [8, 9], industrial applications like hoists, conveyors [10, 11].

The renewable energy resources like wind and solar are using this MLI topologies for micro-grid applications [12-14]. Also, the FACTS devices are widely using this technology for voltage, current compensation, loss reduction, stability improvement and overall performance improvement [15-18].

The single source converters are neutral-point converter and flying capacitor type converters [19-22]. The multi-source inverters are cascaded H-bridge inverter and topologies with and without H-bridge symmetric and asymmetric inverter [23-28]. The H-bridge inverter topologies include T-type, Nilkar, cris-cross, reversing voltage, series connected switched sources, two switched enabled level generation, modular multi-level are recent and more popular type symmetrical MLI [5]. Among symmetrical without H-bridge topology, Mokhberdoran, Babaei, Packed U-Cell, Cascaded Bipolar Switched Cells and Cross Connected Sources MLI are recently developed configurations for medium voltage and advanced control applications [29, 4].

The MLI control schemes are classified mainly based of two classes, fundamental frequency and high switching frequency MLI [30-34]. Among fundamental frequency MLI control scheme, selective harmonic elimination (SHE), space vector pulse width modulation (SVPWM) and Staircase with Fixed Time Step Modulation using Fourier schemes and other techniques [35 and 36]. The Hybrid Modulation Techniques, SVPWM, MCPWM, LSPWM and PDPWM are most famous control schemes for high frequency switching schemes [37, 42, 43].

The paper mainly discusses the multilevel inverter (MLI) configurations and respective control schemes based on the existing literature and new applications. A complete study is done for generalized and hybrid multilevel inverters (MLI). The most accurate control techniques and its applications are discussed in the next sections based on their configurations.

The key features of our work are as follows:

- With the output voltage and power ratings can be increased as number of levels increases. Therefore, the voltage level increasing involves few switching elements to each phase.
- With increase in levels of voltage, harmonic content decreases and hence THD decreases. So, filters required is decreased which will further reduce the cost, maintenance and other factors.

- More free switching angles are observed when additional voltage level increases, hence reselected for harmonic elimination.
- The switching losses will be minimized when adopting advanced PWM techniques like SVPWM, MCPWM and PDPWM etc. techniques.
- The output inverter voltage with fundamental frequency is set fixed by the dc link bus voltage V_{dc}, and is controllable by controlling the variable dc link voltage.

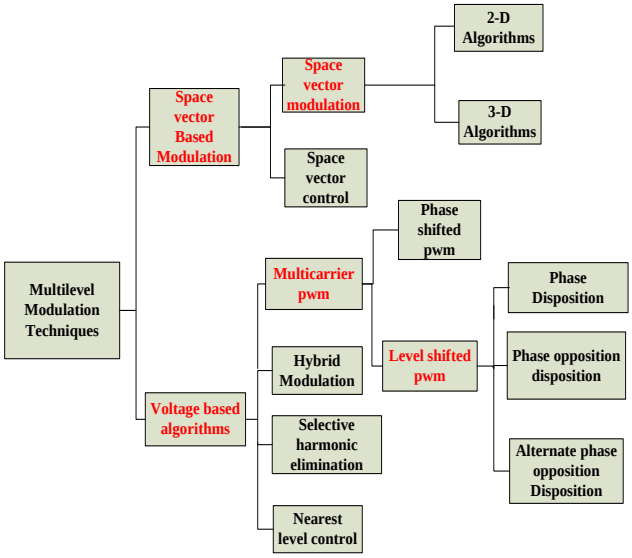

Fig.1: Multilevel Modulation Methods

II. MODULATION STRATEGIES

The fundamental and high frequency based MLI are two types of modulation strategies. In the fundamental frequency based MLI, more inverting units are simply added to generate the switching signals and hence staircase voltages are produced. The selective harmonic elimination (SHE) technique proposed in 1973 produces switching angles to form a fundamental output waveform signal and will eliminate the lower order harmonics. The SHE is mostly used in open loop operation and is one of the most famous techniques for MLI operation for industrial application. In high frequency switching frequency multi-carrier PWM (MCPWM) is classified in terms of phase shifted pulse width modulation (PWM) and level shifted carrier disposition carrier PWM. Similarly, another high frequency switching frequency technique are Hybrid Modulation Techniques (H-PWM), Improved PDPWM with lower and higher carrier cells with phase opposition and alternate hybrid PWM are used for FACTS and industrial load applications.

Different modulation methods are present that are mainly classified as fundamental frequency PWM based and other is higher switching frequency based PWM, later they have their sub-classification. Multilevel modulation is one which is most commonly used for multilevel inverters, as it is easily implemented to low voltage modules.

A reference sinusoidal signal is compared with a reference sinusoidal signal using medium or higher frequency triangular signal to generate multilevel modulation method. The instant was reference greater than carrier the output is '1' and a positive pulse is generated and if reference signal is lower than carrier the output becomes '0' and a negative pulse is generated. This multilevel modulation is further divided into space vector-based pulse width modulation (PWM) and voltage level based PWM. The space vector PWM (SVPWM) is better than sinusoidal PWM because of better bus utilization is provided. However, this method will not provide alternative to capacitor imbalance as this will use narrow pulse width modulation approach. Hence, voltage-based algorithms are widely used with multiple carrier PWM technique as this is providing better output voltage waveforms to meet the desired output power ratings. The literature states that multiple carrier PWM (MCPWM) method will offer 78.5% linear modulation range for achieving maximum output rms voltage. Multiple carrier method has two types in it. 1) Phase Shifted PWM, 2) Level Shifted PWM

2.1 Phase shifted PWM:

In this method carrier signals having phase shift is provided for every pair of switches. The (m-1) levels triangular carriers are necessary for a MLI of 'm' level. The frequency and peak to peak amplitude are fixed for all the carrier triangular waves and any two adjacent carrier triangular signals have a phase shift (φ_{cr}) between them is given by $\varphi_{cr}= 360/(m-1)$.

The phase shifted technique is depicted in below Fig.2.

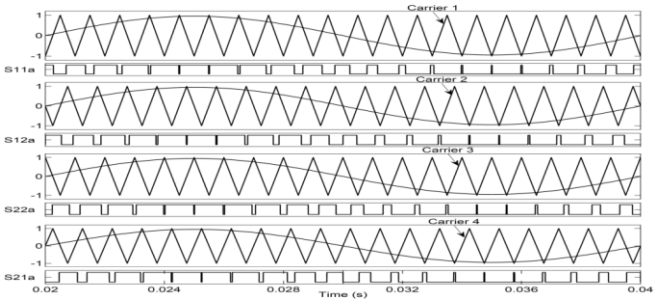

Fig.2: Phase shifted PWM

2.2 Level Shifted PWM:

In this method also carrier signal for each pair of switch will have (m-1) triangular carrier signals which will be needed for a MLI of 'm' level. Similar to the above method also, the frequency and peak to peak amplitude are fixed for all the carrier triangular waves and any two adjacent carrier triangular signals. However, these triangular carrier signals are vertically inclined so that the bands which will be occupied are adjoining. In this level-shifted PWM modulation, controller is designed providing an advantage of the rotating carrier concept. Hence, this applies the same rotating carrier task to every inverter. This level shifted PWM has three types in it. They are given as follows

1) Alternate phase opposition and disposition.

2) Phase opposition disposition.

3) Phase disposition.

2.2.1 Phase Disposition (PD):

In the phase disposition (PD) based modulation technique uses the principle of carriers which uses phase crossways. All the carriers will be placed above and below the zero-orientation line point for the same phase. PDPWM which is the extensively used control scheme for Modular MLI as it provides load voltage and current output waveforms with lower THD. The phase disposition pattern is shown in Fig.3.

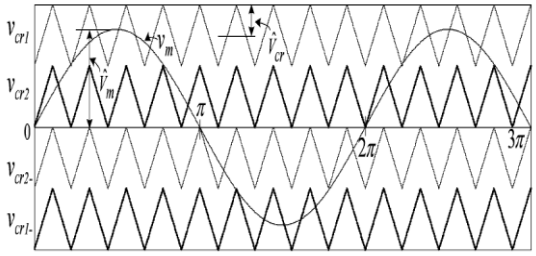

Fig.3: Phase disposition pattern

2.2.2 Phase Opposition Disposition (POD):

Recent advances in multilevel inverters make development of various modulation techniques. The PODPWM is popularly used control strategy for multilevel converters as it provides lower harmonic distortions in load voltage and current. In this POD, the carrier signals are placed above the reference zero-point signal. This will be 180^o out of phase with the carrier signals below and above the reference line parameter. When refereeing to the Fig. 4, the reference signals above will be in phase with different magnitude levels and similarly the carrier signals below will be in-phase with each other below this reference. Hence, these signals will be in phase opposition to the respective levels and hence are 180^o phase shifted. Each pair of carrier signals above and below the reference point will have same frequency and with respective equal amplitude levels. The pattern of phase opposition disposition is shown Fig.4.

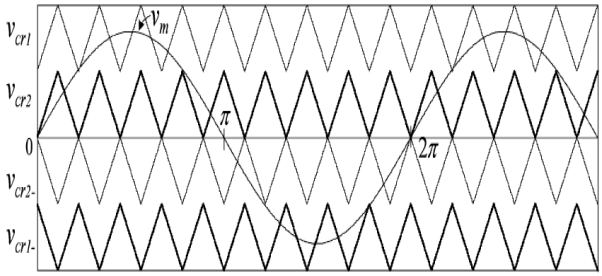

Fig.4: Phase opposition disposition pattern

2.2.3 Alternative Phase Opposition Disposition (APOD):

APOD topology is a level shifted PWM in multi carrier PWM technique in which level shifting of pulses are done by alternative opposition and disposition of phases is shown in Fig.5. It is a voltage-based algorithm in multilevel modulation topology. Its design and implementation is easy when compared to space vector modulation. APOD gives good switching instants with reduced THD level when compared to other conventional PWM techniques. The APOD requires (n-1) carrier waveform where n is the level of phase waveform. The carriers are displaced by 180^0 phase alternatively.

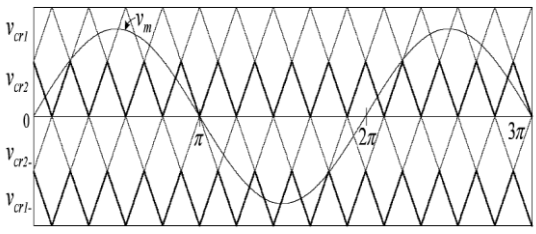

Fig.5: Alternative phase opposition disposition

III. MULTI-LEVEL INVERTER TOPOLOGIES

Wide usage of power electronic inverters with multilevel operation extends the generation range. MLI application in PV system reduces the harmonic content to appreciable limit. As the conventional two-level inverter involves global efficiency and higher THD which leads to the development of MLI structure. To achieve a reliable and effective multi-level inverter output voltage to a medium voltage grid application utilization of MLI is the best approach. Apart from this, dc link inverter voltage is restricted using the switching power electronic devices, voltage ratings for the series connection may not be a problematic. The switching devices are needed to increase the dc link capacitor and switching blocking voltage. Using series link, the maximum permissible switching frequency is lowered to a considerable level. So, the THD reduction will be more complicated. In the view point from THD prospective, harmonic reduction and elevated DC link voltage level using MLI approach is found to be the mainly capable substitute. Compared to a conventional two-level H- bridge inverter of same rating and with same switching frequency, the three level and above stepped multi-level inverter will have better THD, controllability, voltage blocking characteristics and efficiency. A single IGBT or MOSFET switch is carrying only an order of fraction of the dc-link supply or capacitor voltage., therefore voltage stress on these switching devices are decreased effectively. Hence, such MLI configuration is in general used for high rating and better performance requirement applications such as extra-high voltage AC transmission (EHVAC), medium or high voltage ac motor drive systems, HVDC transmission systems, or FACTS devices or micro-grid etc.

3.1 Multilevel Inverter Concept:

Now considering three phases multi-level inverter system into consideration for analysis, with a dc voltage source as input power supply and are connected to dc bus capacitors in series for the inverter. These offer some nodes such that the multi-level inverter is connected and hence each capacitor has an equal voltage across each element, which can be represented as in equation (1) as [1, 2]

$$Vc = \frac{Vdc}{(n-1)} \quad (1)$$

The number of levels is represented with '*n*' for the MLI considered. In this, the term 'level' indicates the nodes number for the MLI are available. An '*n*-level' MLI will have (*n*-1) number of capacitors as described in Fig.6.

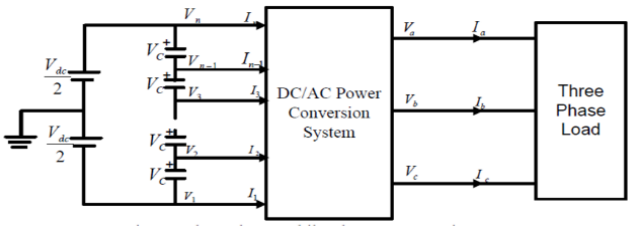

Fig.6 : DC to AC inverter power conversion topology

The output voltage across output terminals of the MLI for any one phase to the ground is denoted by n as depicted in Fig. 7 below. Further, input node voltages and currents are referred to the input voltage terminal of the MLI with reference to the phase-ground. This Fig. 7 is for a five-level output phase to ground voltage of the MLI.

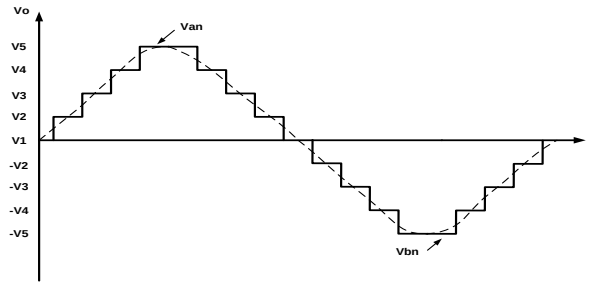

Fig.7: Five Level Output Voltage of The Inverter

3.2 Types and configuration topologies of Multilevel Inverter

In general, the MLI is classified into three different topologies such as diode clamped inverter, flying-capacitor inverter and cascade H-bridge inverter. Diode clamped inverter is most widely used inverter topology for low level applications, but when the level get increases it suffers with voltage balancing of dc-link capacitors. Later, flying capacitor multilevel topology is developed. This topology is also having capacitor voltage balancing problem and it requires a greater number of capacitors. Earlier cascade H-bridge topology is developed. To extend the generation range and to lessen the level of THDs in the PV system output, power electronic inverters are used widely.

3.2.1 Diode Clamp configuration based MLI:

A diode clamped n-level multi-level inverter will have (n-1) number of capacitors on the dc bus link side to generate n levels on the phase voltage to ground reference. A three phase five-level diode clamped MLI configuration is depicted in Fig.8. The DCMLI model is foremost developed model which is suitable effectively for PV system utilization.

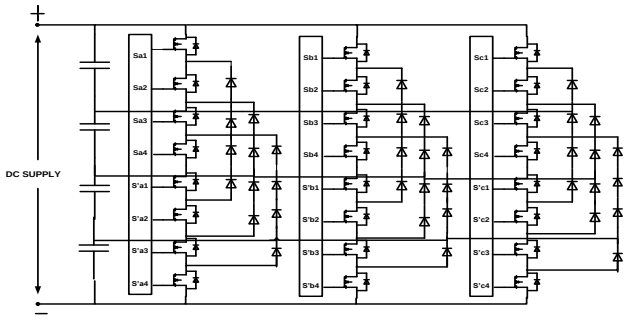

Fig.8 Three Phase Five-Level DCMLI Topology

For each phase for a three-phase output application for the MLI share a common DC bus link voltage which will be alienated into five levels by the (5-1=4) four DC bus capacitors. The dc bus will have four capacitors named as C_1, C_2, C_3, and C_4. The first capacitor on the top is specified as C1, next below it is C2 and the third one from the top capacitors is C3 and the bottom capacitor is C4. The middle capacitor C_2 and C_3 will act like a neutral point of inverter and helps in improving the switching ON/OFF characteristics with neutral point as base or reference parameter. Hence, a five stepped voltage output will be produced with the help of these four capacitors. The C2 and C1 will help in producing positive voltage with C2 across switches conducts first and will develop a step voltage, later these switches will be off and capacitor C2 voltage is blocked and immediately C1 and switches across it will conduct, but with upper voltage threshold values creating another voltage step, but with lesser period of operation. Hence, two stepped positive voltage steps are produced. In the similar fashion C3 will conduct first will produce negative side voltage step and then wit will be off and then C4 will be conducted to get negative stepped voltage. Hence, five stepped or five level voltage is formed with this topology. The conducting characteristics will be improved with the help of these unidirectional switches. The voltage across each capacitor will be $V_{dc}/4$ ideally and the switching stress on each switching device like IGBT or MOSFET or so is limited to V_{dc} from end to end of the clamping diodes. A major mechanism is that, it will vary with this topology from a generalized two-level inverter are clamping diodes.

3.2.3 Flying Capacitor Multilevel Inverter:

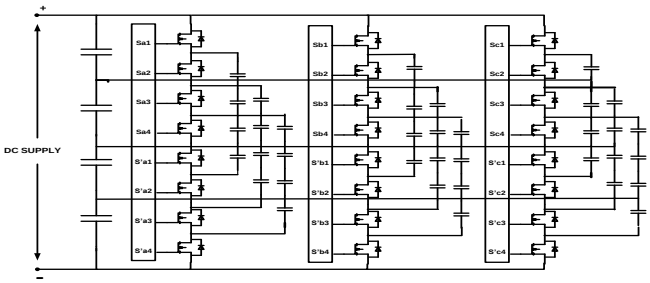

Fig.9: A Three-Phase Five-Level FCMLI Topology

The flying capacitor clamped multilevel inverter (MLI) engage in the use of extra clamped capacitors to these power switches like IGBT or MOSFET or so in the phase rail to offer the DC voltage level. This structure permits the inverter to provide high potential particularly during power outages because of the redundancy in switching states afforded by the flying clamping capacitor. In this flying capacitor type MLI configuration, the inverter in each phase leg will have an identical arrangement. The voltage level for the flying-capacitors MLI is analogous to that of the diode clamped MLI for the same level of output voltage is considered. A 3Φ five-level flying capacitor MLI configuration is depicted in Fig.9. It shows that eight switches in each phase and numbering order is different from the diode clamped multi-level inverter. The numbering is of no importance providing the switches which are to be turned on and off in the accurate sequence to generate the desired output voltage.

3.3.3 Cascaded Multilevel Inverter:

Another multilevel inverter (MLI) topology for a lower power device requirement when contrasted to earlier discussed configuration is called as cascaded H-bridge multilevel inverter (CHB-MLI). In this configuration, the input dc source voltage is from a fixed source such as controlled PV cell, battery or capacitor or such dc sources.

At one time S1 and S2 will conduct and produce a positive voltage and the same direction current. In another half cycle, these two switches will be off and S3 and S4 will be turned on creating a negative side voltage with this negative side current. Hence, ac voltage is produced easily using appropriate PWM pulse technique.

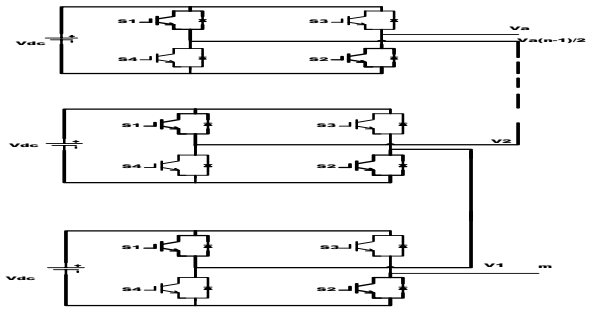

Fig.10: A Single Cascaded H-Bridge

There will be single dc power sources in each H-bridge leg and hence multiple dc input power sources are used for each step of voltage. In this three stepped seven level cascaded H-bridge configuration, first bottom positive S1 and S3 will be on, after some time these two will be off and immediately middle S1 and S2 will be at above voltage level of the earlier bridge and will operate lesser time than this. Finally, top two S1 and S2 switches will be on and the middle two switches' will be off. Hence a three stepped positive seven level voltage is produced with s1 and S2. In the similar way, the S3 and S4 from the bottom to top H-bridges are on to produce negative voltage steps. Based on this phenomenon, CHB-MLIs have also been anticipated with sources like fuel cell supply or photovoltaic arrays so as to attain higher levels. Thus, the resultant AC output inverted voltage is produced by the adding up of the voltages produced by various H-bridge cells. The general structure of a single-phase cascaded H-bridge with individual dc supply is shown in Fig. 10.For every individual dc supply is connected to the H-Bridge multi-level inverter (MLI), the ac terminal output inverted voltage obtained from the various level inverters is series connected. In the cascaded MLI, it is not necessary to use clamping diodes or use of any voltage balancing capacitors such as diode clamped or capacitor clamped multi-level inverters and the component details based on 'n'-level is given in Table 1.

Table 1: Power Components of Inverter Topology

Power Component	Inverter Topology		
	DCMLI	FCMLI	Cascaded H-Bridge
Main Switching device	2(n-1)	2(n-1)	2(n-1)
Flying capacitors	0	$\frac{(n-1)(n-2)}{2}$	0
Clamping diodes	(n-1)(n-2)	0	0
DC bus capacitors	(n-1)	(n-1)	$\frac{(n-1)}{2}$
Anti-parallel diodes	2(n-1)	2(n-1)	2(n-1)

Merits:

1. Since all these switches are controlled (ON or OFF) at fundamental frequency, therefore its efficiency is higher than a conventional converter topology.
2. Practical implementation is not complicated and misfiring or fire through type power electronic switch failures will also not that influenced as in conventional converters.

Demerits:

3. As the number of levels increases, excessive clamping diodes are necessary.
4. Independent real and reactive power flow control with individual converter is complex in a multi-level inverter system.
5. Capacitor voltage unbalance for higher levels.

IV. SIMULATION RESULTS

In this section, sinusoidal PWM (SPWM) of 2.0 kHz frequency is used as the basic modulation method for cascaded H-Bridge inverters from three levels to thirty-one level are discussed. Initially, it is studied and compared with three and five level inverters. The dc source considered here in the case study is 350V and each capacitor rating is 2200µF is used with H-Bridge converters. The performance of the three-level to thirty-one level multilevel inverters are evaluated constant three phase balanced RL load of 1KW and 100KVAR are analyzed. The software used for study is MATLAB/ SIMULINK. The operation of sinusoidal pulse width operation is, the produced sine wave is compared with carrier based triangular wave. If the sine wave inverter voltage magnitude is more than carrier triangular wave, then pulses will be generated, otherwise no pulses are produced and hence no switch-on pulse signal is given to the switch. The switching pulse signal is given to respective IGBT switch to get controlled output voltage waveform. The MATLAB based simulation of multilevel inverter up-to thirty-one levels are discussed in this section.

4.1 Case 1: Three and Five level Cascaded H-bridge Multi level Inverter

A 3Φ cascaded H-bridge multi-level inverter (CHBMLI) type three levels inverter for a multi carrier having a single reference modulation topology is depicted in Fig. 11(a). The five-level inverter with cascaded H-bridge configuration is shown in Fig.11(b). The rating of capacitor which is placed across the load is 2200 micro farads and input dc voltage considered in this work is 30V and the expected output AC voltage is 60V Ph-N. The Fig. 11(b) describes the model of five-level cascade H-bridge inverter for a single A-phase. Similar two identical circuits will be for the B and C phases. When considering the five-level inverter, during the positive half cycle, the top bridge Sa21 and Sa24 will be conducting for a period of α seconds and then the bottom second bridge positive switches Sa11 and Sa14 will be on without switching off Sa21 and Sa24. Here, these two switches will be conducting along with Sa11 and Sa14 to get medium and high voltage applications,

otherwise the top bridge circuit switches can be off. In the same way, the negative waveform is obtained with the negative switches as discussed earlier. The sum of these voltages across the pair of switches will give the peak to peak voltage of the MLI. The number of voltage levels can be given by (2s+1) with 's' number of switches. So, 2 sources are in five level, hence 5 level voltage and single source for three level, so three level voltage is obtained as in Fig. 12(a) and Fig. 12(b).

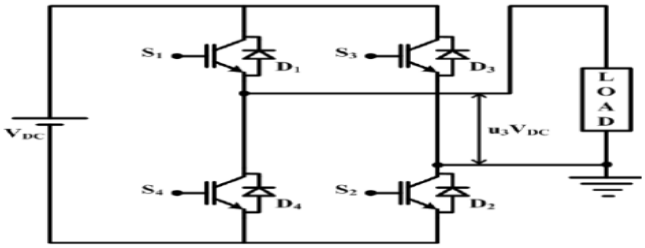

Fig. 11(a) Three-phase 3-level Cascaded H-bridge Multi level inverter

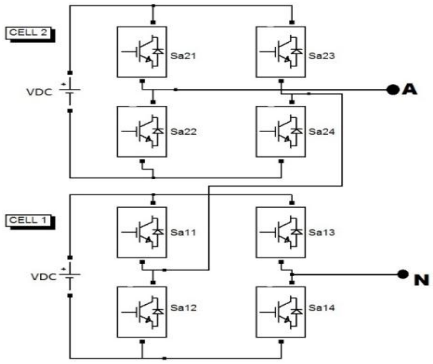

Fig.11(b) 5-level Cascaded H-bridge Multi level inverter

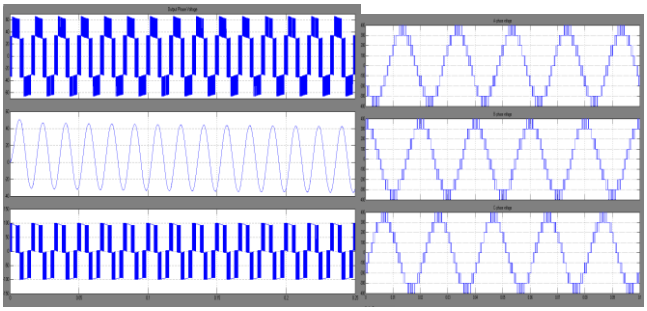

Fig.12(a) 3-level output Phase voltages
Fig.12(b) 5 level CHB-MLI

Three phases cascaded H-bridge configuration of a three and five level inverter employing various multi carrier single reference modulation techniques. The sub-figures for this figure are shown similar to the one produced with flying capacitor type design. The capacitor rating is 2200 micro farads and input DC voltage is 30V and output AC is 62V Ph-N. In this figure top part shows, phase to neural voltage and is 62Volts peak and middle part of figure is for current which is 40A peak and the bottom figure shows phase to phase voltage nearly 100 Volts. Figure 13(a) depicts MATLAB/ Simulink based output model of five-level H-bridge inverter. A discrete three phase programmable source gives reference sinusoidal voltages based on the prescribed frequency and amplitude. The sub-system at the bottom of this Fig. 13(a) will give carrier signal waves for all the six bridges. When the sinusoidal waveform is compared with the carrier triangular or saw-tooth waveform and the former is more in amplitude, pulse is produced for the respective switch. As discussed earlier, stepped waveform is produced with the delayed waveform which is programmed in this sub-system. Hence, this cascaded H-bridge converter will give better sinusoidal waveform than the earlier methods. This topology also do not require, flying-capacitors or diodes, hence elements cost is reduced and therefore reliability and efficiency is improved. Natural 3n harmonics is cancelled even for a single-phase circuit due to (2s+1) characteristics.

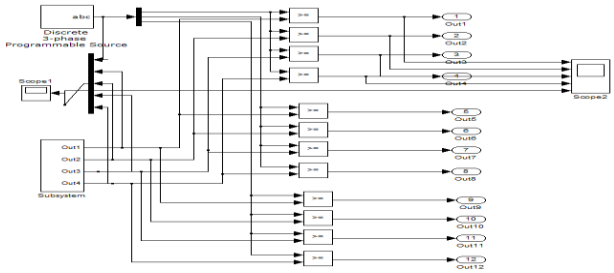

Fig.13(a) Design of modulator block of SPWM controlled 5-level inverter

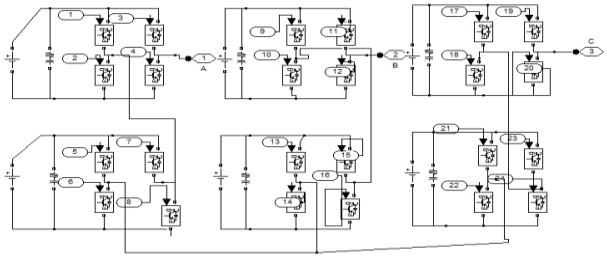

Fig.13(b) Sub system of Three-phase five-level cascaded H-bridge MLI

4.2 Case 2: 13-level Cascaded H-bridge Multilevel Inverter

The Fig. 14 describes the MATLAB/ Simulink based design of thirteen level inverter. Each sub-block consists of one H-bridge circuit and hence five sub-blocks are used in each phase to get the desired thirteen level inverter. All the H-bridge circuits are connected in series and each is supplied with an individual voltage source. The open loop control circuit can also be seen on the Fig.14 at the right side. In the place of programmable voltage source, if the phase-locked loop-based voltage at the point of common coupling (PCC) reference value gives the closed loop control with reference and actual error controller loop block. This closed loop will give better controllability, but it increases the control circuit design complexity.

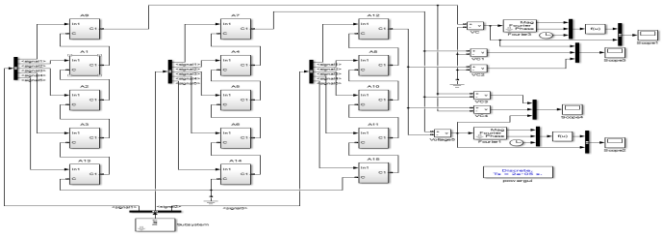

Fig.14 Simulink model of thirteen-phase thirteen-level cascaded H-bridge MLI

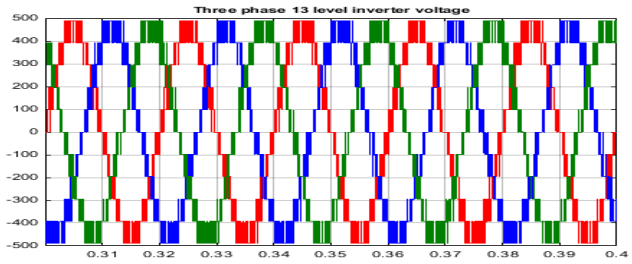

Fig. 15(a) Output Phase-ground voltages of 13-level CHB-MLI

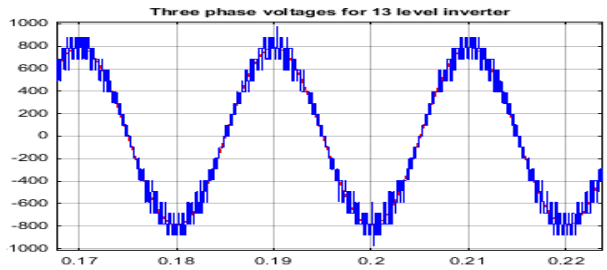

Fig. 15(b) line voltages of 13-level CHB-MLI

The phase-ground (phase voltage) of thirteen level voltage source inverter are shown in Fig. 15(a) and phase-phase or line voltage of the same system is shown in Fig.15 (b). There will be increased sinusoidal nature of the waveform with the thirteen-level compared to earlier 5-level inverter. Hence, THD, voltage level and performance is increased with this thirteen level inverter compared to 5 or three level inverter. The THD value is 6.88% with thirteen level inverter, whereas with five-level, the THD is 36.1% and with three level is 42.3% THD. Hence a considerable decrease in THD is observed with thirteen-level inverter. The results with the thirteen-level inverter with CHBMLI is better than the work with [22]

4.3 Case 3: 15-level Cascaded H-bridge Multilevel Inverter

In the 15-level inverter, there will be an additional one sub-block with a H-bridge converter will be present compared to thirteen level inverter. Also, there will be two steps in the voltage waveform is observed in positive side for a 15-level inverter than a 13-level inverter as shown in Fig.16(a) and Fig.16(b). The phase and line voltages are shown in these figures respectively. The THD value for the 15-level inverter is 5.17%. The 15 or 13-level inverter holds good for renewable energy resources grid integration for a micro-grid network or for motor drive control applications.

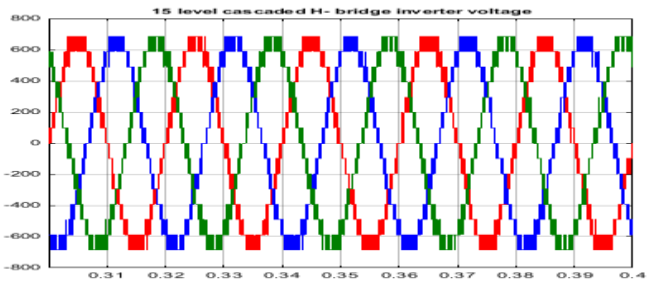

Fig.16(a) Output Phase-ground voltages of 15-levelCHB-MLI

Fig.16(b) phase voltages of 15-level CHB-MLI

4.4 Case 4: 21-level Cascaded H-bridge Multilevel Inverter

The 21-level output phase voltage waveform is shown in Fig.17(a), using level shifted or phase disposition (LS or PD PWM) pulse width modulation technique is shown in Fig.17(b). There are four critical voltages shown in Fig.17(b) is for 5 level inverter and for 21-level, there will be 10 such critical voltages with different amplitudes but with same frequency of operation. Under such switching scheme, we will be getting stair-based steps in the voltage with better waveform and THD value of 2.91%.

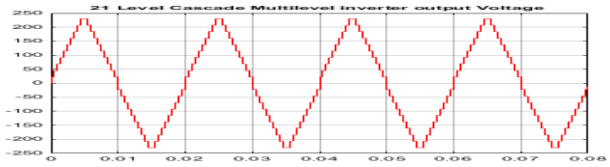

Fig.17(a) phase voltages of 21-level CHB-MLI

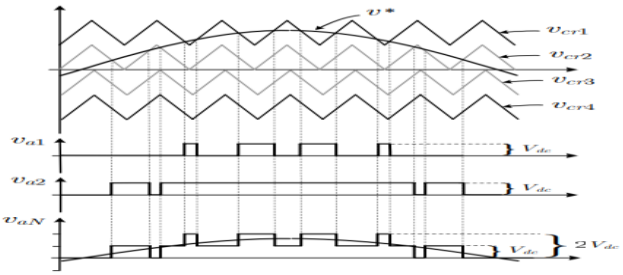

Fig.17 (b) PDPWM technique

4.5 Case 5: 31-level Cascaded H-bridge Multilevel Inverter

The 31-level CHBMLI control circuit for three phase system using MATLAB/ Simulink is shown in Fig.18In this it is observed that 15 carrier voltage references with the same frequency, but with different turn-on values and amplitudes respectively. These carrier wave signals are compared with the reference sinusoidal signal to get the desired pulses and with steps type waveform like a stair case. In this there will be four different stages of input sources with 24 volts dc, 14V, 96V, and 192 volts respectively to achieve this 31-stair stepped waveform. The same PDPWM based pulse generation technique is also applied for this topology. The voltage and phase current for the 31-level inverter is shown in Fig.19. It can be observed that the voltage and current are in-phase with each other and hence almost unity power factor operation is obtained. The THD value with the proposed control scheme for the 31-level inverter is 2.57%. The blocking voltage is increased and hence load handling capacity is increased. Real and reactive independent control is possible with higher efficiency and better reliability is possible.

It can further be concluded that, the THD value is decreasing as the level of voltage steps is increasing.

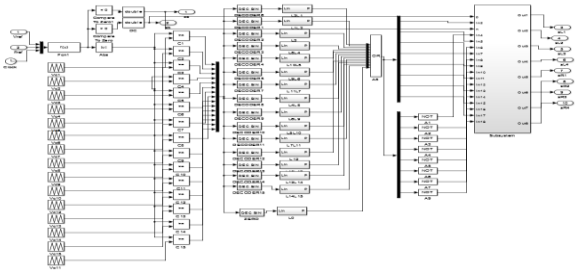

Fig.18 Simulink model of three-phase thirty-one level cascaded H-bridge MLI

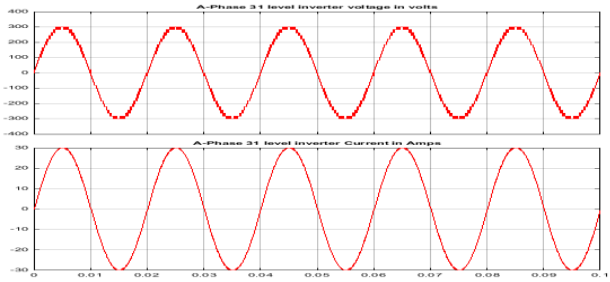

Fig.19 Output Phase-ground voltages and current of 31-level CHB-MLI

V. RESULTS AND DISCUSSION

Simulation circuit and results for three level in Figure 11(a) and 12(a), five level from Fig.11(b), 12(b), and 13, thirteen level in Fig.14 and 15, fifteen level in Fig.16, twenty-one level in Fig. 17 and thirty-one level inverters in Fig.18 and 19 are shown respectively. And the total harmonic distortion for each inverter is shown in Table 2.

TABLE 2 Voltage THD of three, five, thirteen, fifteen, twenty-one and thirty-one level inverters

Multilevel Inverter	Three Level Inverter	Five Level Inverter	Thirteen Level Inverter	Fifteen Level Inverter	Twenty-one Level Inverter	Thirty-one Level Inverter
THD for voltage	46.3%	36.1%	6.88%	5.17%	2.91%	2.57%

VI. CONCLUSION

This paper discusses the design and modeling of various basic multilevel inverter circuit configurations with their control schemes. Different applications using various inverter networks are also shown. Multilevel inverter (MLI) produced more concentration from its evolutions to its present decade due to its added merits in high power applications with low switching on or off frequency and lower THD. Here, the MLI is modeled using three different configurations like, diode clamped MLI, flying capacitor based MLI and cascaded H-bridge topology. A continuous sinusoidal pulse width modulation (CSPWM) strategy is employed to control the inverter effectiveness as CSPWM control technique is more popular in industrial motor load control applications due to its harmonic reducing capability when several phase shifting options on carrier signals are applied. The MATLAB based simulation is done and is shown that as the number of voltage level increases, and hence produces higher voltage with lesser THD value. It is simple to conclude that multilevel inverter (MLI) research and development action are practiced in an explosive growth rate. A trend of having progressively multilevel inverters is obvious because of these advantages. The total harmonic distortion for each level is calculated and compared.

The simulation of three level, five level, thirteen, fifteen, twenty-one and thirty-one level inverters are realized in MATLAB SIMILINK where for switching of the ideal diode sine pulse width modulation (SPWM) is used for modulation purpose Phase opposition disposition (POD) carrier scheme is used. From the different levels of simulation, it is clear that THD can be decreased by increasing number of levels.

REFERENCES

1. Prabaharan, Natarajan, and Kaliannan Palanisamy. "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications." *Renewable and Sustainable Energy Reviews* 76 (2017): 1248-1282.
2. Noman, Abdullah M., Abdullrahman A. Al-Shamma'a, Khaled E. Addoweesh, Ayman A. Alabduljabbar, and Abdulrahman I. Alolah. "A survey on two level and cascaded multilevel inverter topologies for grid connected PV system." In *IECON 2017-43rd Annual Conference of the IEEE Industrial Electronics Society*, pp. 2369-2376. IEEE, 2017.
3. Benbouhenni, Habib, Zinelaabidine Boudjema, and Abdelkader Belaidi. "Indirect vector control of a DFIG supplied by a two-level FSVM inverter for wind turbine system." *Majlesi Journal of Electrical Engineering* 13, no. 1 (2019): 45-54.
4. Vijeh, Mahdi, Mohammad Rezanejad, Emad Samadaei, and Kent Bertilsson. "A general review of multilevel inverters based on main submodules: Structural point of view." *IEEE Transactions on Power Electronics* 34, no. 10 (2019): 9479-9502.
5. El-Hosainy, Asmaa, Hany A. Hamed, Haitham Z. Azazi, and E. E. El-Kholy. "A review of multilevel inverter topologies, control techniques, and applications." In *2017 Nineteenth International Middle East Power Systems Conference (MEPCON)*, pp. 1265-1275. IEEE, 2017.
6. Chattopadhyay, Sumit K., and Chandan Chakraborty. "Full-Bridge Converter With Naturally Balanced Modular Cascaded H-Bridge Waveshapers for Offshore HVDC Transmission." *IEEE Transactions on Sustainable Energy* 11, no. 1 (2019): 271-281.
7. Adam, Grain Philip, Islam Azmy Gowaid, Stephen Jon Finney, Derrick Holliday, and Barry W. Williams. "Review of dc–dc converters for multi-terminal HVDC transmission networks." *IET Power Electronics* 9, no. 2 (2016): 281-296.
8. Yadav, Apurv Kumar, K. Gopakumar, Loganathan Umanand, Kouki Matsuse, and Hisao Kubota. "Instantaneous balancing of neutral-point voltages for stacked DC-link capacitors of a multilevel inverter for dual-inverter-fed induction motor drives." *IEEE Transactions on Power Electronics* 34, no. 3 (2018): 2505-2514.
9. Kirankumar, B., YV Siva Reddy, and M. Vijayakumar. "Multilevel inverter with space vector modulation: intelligence direct torque control of induction motor." *IET Power Electronics* 10, no. 10 (2017): 1129-1137.

10. Khanal, Saroj, and Vahid R. Disfani. "Reduced Switching-Frequency Modulation Design for Model Predictive Control Based Modular Multilevel Converters." *arXiv preprint arXiv:1912.08433* (2019).
11. Shanono, Ibrahim Haruna, Nor Rul Hasma Abdullah, and Aisha Muhammad. "A survey of multilevel voltage source inverter topologies, controls, and applications." *International Journal of Power Electronics and Drive Systems* 9, no. 3 (2018): 1186.
12. Rojas, Christian A., Samir Kouro, Marcelo A. Perez, and Javier Echeverria. "DC–DC MMC for HVdc grid interface of utility-scale photovoltaic conversion systems." *IEEE Transactions on Industrial Electronics* 65, no. 1 (2017): 352-362.
13. Chattopadhyay, Sumit K., and Chandan Chakraborty. "A new asymmetric multilevel inverter topology suitable for solar PV applications with varying irradiance." *IEEE Transactions on Sustainable Energy* 8, no. 4 (2017): 1496-1506.
14. Wang, Tianzhen, Jie Qi, Hao Xu, Yide Wang, Lei Liu, and Diju Gao. "Fault diagnosis method based on FFT-RPCA-SVM for cascaded-multilevel inverter." *ISA transactions* 60 (2016): 156-163.
15. Ananth D. V, Kumar Y. N, Tilak B. B. G, Raghunath P. S.: Multi-level inverters and its application of statcom using svpwm and spwm techniques, IOSR Journal of Electrical and Electronics Engineering (IOSRJEEE), (2012), vol. 2 no 5, pp. 30-38.
16. Prabaharan, Natarajan, and Kaliannan Palanisamy. "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications." *Renewable and Sustainable Energy Reviews* 76 (2017): 1248-1282.
17. Farias, João Victor Matos, Allan Fagner Cupertino, Victor De Nazareth Ferreira, Heverton Augusto Pereira, Seleme Isaac Seleme Junior, and Remus Teodorescu. "Reliability-Oriented Design of Modular Multilevel Converters for Medium-Voltage STATCOM." *IEEE Transactions on Industrial Electronics* (2019).
18. Yuan, Yubo, Peng Li, Xiangping Kong, Jiankun Liu, Qun Li, and Ye Wang. "Harmonic influence analysis of unified power flow controller based on modular multilevel converter." *Journal of Modern Power Systems and Clean Energy* 4, no. 1 (2016): 10-18.
19. Yadav, Apurv Kumar, K. Gopakumar, Loganathan Umanand, Kouki Matsuse, and Hisao Kubota. "Instantaneous balancing of neutral-point voltages for stacked DC-link capacitors of a multilevel inverter for dual-inverter-fed induction motor drives." *IEEE Transactions on Power Electronics* 34, no. 3 (2018): 2505-2514.
20. Lee, Sze Sing, and Kyo-Beum Lee. "Dual-T-type seven-level boost active-neutral-point-clamped inverter." *IEEE Transactions on Power Electronics* 34, no. 7 (2019): 6031-6035.
21. Lei, Yutian, Christopher Barth, Shibin Qin, Wen-Chuen Liu, Intae Moon, Andrew Stillwell, Derek Chou et al. "A 2-kW single-phase seven-level flying capacitor multilevel inverter with an active energy buffer." *IEEE Transactions on Power Electronics* 32, no. 11 (2017): 8570-8581.
22. Barth, Christopher B., Pourya Assem, Thomas Foulkes, Won Ho Chung, Tomas Modeer, Yutian Lei, and Robert CN Pilawa-Podgurski. "Design and control of a GaN-based, 13-level, flying capacitor multilevel inverter." *IEEE Journal of Emerging and Selected Topics in Power Electronics* (2019).
23. Vemuganti, Hari Priya, Dharmavarapu Sreenivasarao, and Ganjikunta Siva Kumar. "Zero-sequence voltage injected fault tolerant scheme for multiple open circuit faults in reduced switch count-based MLDCL inverter." *IET Power Electronics* 11, no. 8 (2018): 1351-1364.
24. Garapati, Durga Prasad, V. Jegathesan, and Moorthy Veerasamy. "Minimization of power loss in newfangled cascaded H-bridge multilevel inverter using in-phase disposition PWM and wavelet transform based fault diagnosis." *Ain Shams Engineering Journal* 9, no. 4 (2018): 1381-1396.
25. Narendran, A., and R. Sureshkuma. "Hysteresis-Controlled-Landsman Converter Based Multilevel Inverter Fed Induction-Motor System Using PIC." *Microprocessors and Microsystems* (2020): 103099.
26. Yang, Wenbo, Qiang Song, Shukai Xu, Hong Rao, and Wenhua Liu. "An MMC topology based on unidirectional current H-bridge submodule with active circulating current injection." *IEEE Transactions on Power Electronics* 33, no. 5 (2017): 3870-3883.
27. Marzoughi, Alinaghi, Rolando Burgos, Dushan Boroyevich, and Yaosuo Xue. "Design and comparison of cascaded H-bridge, modular multilevel converter, and 5-L active neutral point clamped topologies for motor drive applications." *IEEE Transactions on Industry Applications* 54, no. 2 (2017): 1404-1413.
28. Liu, Ying, Rui Fan, Xiaoning Zhang, Zhentao Tu, and Jun Zhang. "Bipolar high voltage pulse generator without H-bridge based on cascade of positive and negative Marx generators." *IEEE Transactions on Dielectrics and Electrical Insulation* 26, no. 2 (2019): 476-483.
29. Meenalochani, K., B. Shanthi, and C. R. Balamurugan. "Performance analysis on bipolar PWM strategies for single phase quasi-Z-source fed seven level modified cascaded H-bridge inverter with asymmetric switched-inductor cell." *International Journal of Engineering & Technology* 7, no. 2.8 (2018): 583-587.
30. Venkataramanaiah, J., Y. Suresh, and Anup Kumar Panda. "A review on symmetric, asymmetric, hybrid and single DC sources based multilevel inverter topologies." *Renewable and Sustainable Energy Reviews* 76 (2017): 788-812.
31. Hajizadeh, Mehdi, and Seyed Hamid Fathi. "Fundamental frequency switching strategy for grid-connected cascaded H-bridge multilevel inverter to mitigate voltage harmonics at the point of common coupling." *IET Power Electronics* 9, no. 12 (2016): 2387-2393.
32. Masaoud, Ammar, Saad Mekhilef, Hew Wooi Ping, and Kiing Ing Wong. "A simplified structure for three-phase 4-level inverter employing fundamental frequency switching technique." *IET Power Electronics* 10, no. 14 (2017): 1870-1877.
33. Raman, S. Raghu, Yat Chi Fong, Yuanmao Ye, and Ka Wai Eric Cheng. "Family of Multiport Switched-Capacitor Multilevel Inverters for High-Frequency AC Power Distribution." *IEEE Transactions on Power Electronics* 34, no. 5 (2018): 4407-4422.
34. Sathik, M. Jagabar, Kaustubh Bhatnagar, Yam P. Siwakoti, Hussain M. Bassi, Muhyaddin Rawa, N. Sandeep, Yongheng Yang, and Frede Blaabjerg. "Switched-capacitor multilevel inverter with self-voltage-balancing for high-frequency power distribution system." *IET Power Electronics* (2020).
35. Barbie, Eli, Raul Rabinovici, and Alon Kuperman. "Analytic formulation and optimization of weighted total harmonic distortion in single-phase staircase modulated multilevel inverters." *Energy* (2020): 117470.
36. Kamani, Piyush L., and Mahmadasraf A. Mulla. "Middle-level SHE pulse-amplitude modulation for cascaded multilevel inverters." *IEEE Transactions on Industrial Electronics* 65, no. 3 (2017): 2828-2833.
37. Devi, B. Gayathri, and B. K. Keshavan. "A novel hybrid Phase Shifted-Modified Synchronous Optimal Pulse Width Modulation based 27-level inverter for grid-connected PV system." *Energy* 178 (2019): 309-317.
38. Chokkalingham, Bharatiraja, Sanjeevikumar Padmanaban, and Frede Blaabjerg. "Investigation and comparative analysis of advanced PWM techniques for three-phase three-level NPC-MLI drives." *Electric Power Components and Systems* 46, no. 3 (2018): 258-269.
39. Mukherjee, Sarbojit, Sayan De, Santomit Sanyal, Suman Das, and Sumit Saha. "A 15-level asymmetric H-bridge multilevel inverter using d-SPACE with PDPWM technique." *International Journal of Engineering, Science and Technology* 11, no. 1 (2019): 22-32.
40. Irusapparajan, G., Periyaazhagar, D., Prabaharan, N. and Jerin, A.R.A., 2019. Experimental verification of trinary DC source cascaded H-bridge multilevel inverter using unipolar pulse width modulation. *Automatika*, *60*(1), pp.19-27.
41. Chokkalingam, Bharatiraja, Mahajan Sagar Bhaskar, Sanjeevikumar Padmanaban, Vigna K. Ramachandaramurthy, and Atif Iqbal. "Investigations of multi-carrier pulse width modulation schemes for diode free neutral point clamped multilevel inverters." *Journal of Power Electronics* 19, no. 3 (2019): 702-713.
42. Jayabalan, Maalmarugan, Baskaran Jeevarathinam, and Thamizharasan Sandirasegarane. "Reduced switch count pulse width modulated multilevel inverter." *IET Power Electronics* 10, no. 1 (2017): 10-17.
43. Shuvo, Shuvangkar, Eklas Hossain, Tanveerul Islam, Abir Akib, Sanjeevikumar Padmanaban, and Md Ziaur Rahman Khan. "Design and hardware implementation considerations of modified multilevel cascaded h-bridge inverter for photovoltaic system." *Ieee Access* 7 (2019): 16504-16524.

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