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# A Low Jitter – Low Phase Noise Wideband Digital Phase Locked Loop In Nanometer Cmos Technology

**Nilesh D. Patel, Amisha P. Nai Priyesh P. Gandhi**

***Abstract - For high speed communication applications; jitter, phase noise and power consumption are most critical parameters required to be considered for PLL designs. A sub harmonically injection locking concept can be used in PLL to reduce jitter and phase noise. Such design is very effective for high frequency applications. This article presents similar design for 7.5-GHz Phase locked loop in 180 nm CMOS technology. The measured phase noise of the proposed PLL with self aligned injection at 1 MHz offset is 121.14 dBc/Hz and rms jitter is 110 fs. The total dc power consumption is 13.99 mW. To support the claim process variation with design corner analysis using random variations are carried out.***

***Keywords-component; CMOS, PLL, Loop Filter, Voltage Control Oscillator, Phase Frequency Detector, Low Pass Filter, Delay Locked Loop***

## I. INTRODUCTION

The Phase Locked Loop is heart of modern wireless DSP and Instrumentation Systems. It is used mainly for synchronization, clock synthesis and skew jitter reduction. It generate clock signal which is to be used as reference signal [1, 2].

There are five different blocks of PLL: Phase Frequency Detector, Chare Pump, Loop Filter, Voltage Controlled Oscillator and Frequency Divider. Recently all digital and analog communication devices operate at very high frequency so a faster locking PLL is needed. Hence there are many challenges to derive architectures of various blocks of PLL [1, 2].

At present most of the researchers are working at system level to develop a cost effective and reliable PLL which gives optimum performance. They are focusing to achieve higher lock range with lower lock time and tolerable phase noise which can be designed as single module on SoC [6].

For high speed communication applications; jitter, phase noise and power consumption are most critical parameters required to be considered for PLL designs.

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* Correspondence Author
**Dr. Nilesh D. Patel*,** Principal M. L. Institute of Diploma Studies Bhandu, India ec.nileshpatel@gmail.com
**Dr. Amisha P. Naik,** Associate Professor, Institute of Technology, Nirma University Ahmedabad, India amisha.naik@nirmauni.ac.in
**Dr. Priyesh P. Gandhi,** Principal Sigma Institute of Engineering Vadodara, India priyeshgandhi@gmail.com



It is generally observed that major sources of phase noise are due to misalignment between VCO, PFD and input reference signal. It is known that phase noise is removed by high pass filter at input, while output of PFD is a low pass response. To design low jitter with low phase noise, the selection of loop bandwidth is most important. The VCO frequency is inversely proportional to phase noise [2, 3, 11]. The quality of a clock signal is heavily dependent on its phase noise and jitter. An ideal clock source would generate a pure sine wave. All signal power would be generated at one frequency. However, actuality all clock signals have some degree of phase modulated noise. This noise spreads the power of the clock signal to adjacent frequencies, resulting in noise sidebands. The phase noise is typically expressed in dBc/Hz and represents the amount of signal power at a given sideband or offset frequency from the ideal clock frequency [3, 4, 5].

A sub harmonically injection locking concept can be used in PLL to reduce jitter and phase noise. Such design is very effective for high frequency applications. The main issues for such design are locking range and phase matching between injected signal and oscillator [7, 8].

This article is focused to provide following merits over the existing designs reported in last decade. The design objective is to minimize the jitter and phase noise which can be integrated with high speed ASIC design. After carrying out thorough literature survey, simulations and analysis, following modifications are done to bring novelty in proposed digital phase locked loop design.

The modified TSPC Logic based D flip flop is designed to build phase frequency detector to reduce dead zone. In addition to that it provides good adaptability.

To improve the current matching characteristics, current mode differential charge pump design is used. This design provides full swing in turn clock signal can handle full swing.

The LC based oscillator is used for Sub Harmonic Injection locking concept to increase the clock speed. It can also provide wide tuning range using various modified blocks discussed. The Delay Locked Loop block is added to achieve desired range with improved noise and jitter performance.

To verify the proposed design the concept proposed the author used Tanner EDA and Mentor Graphics tools to carry out simulations in 180 nm CMOS technology. The proposed digital PLL have very stable high frequency signal output with wide tuning range. It is competent to generate high speed clock signal with minimum low phase noise.

## II. SUB HARMONICALLY INJECTED LOCKED DIGITAL PLL

The basic difference between conventional and Sub harmonically Injected Locked PLL (SILPLL) is shown below Fig. 1 and 2. Here the VCO is replaced by sub harmonically injected VCO. The delay element is also introduced between input and SILVCO. Here DLL is used as a delay element to improve accuracy and jitter performance.

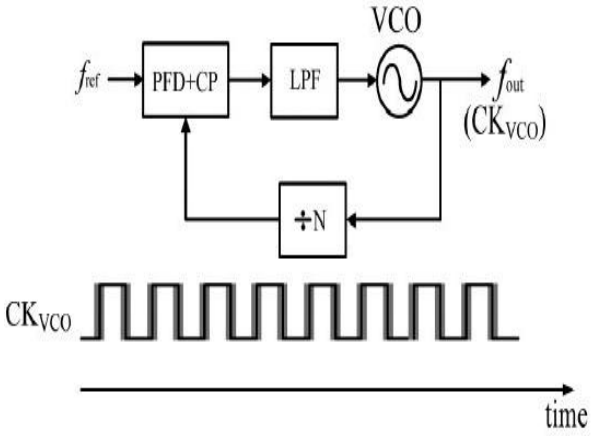


**Fig. 1: Conventional PLL [3]**

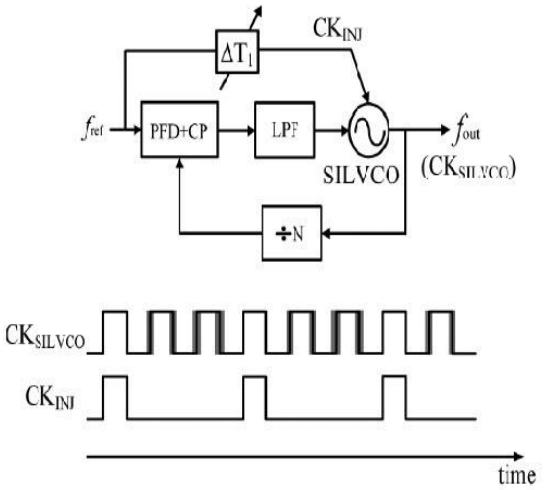


**Fig. 2: Proposed SILPLL [8, 10]**

In conventional PLL, the output phase noise can be reduced using the low phase noise input reference signal. The output waveform with the jitter is shown in Fig. 3. For the conventional PLL and the output suffers from the jitter due to the noise of each building block in the PLL. The block diagram of conventional, SILPLL, its output and reference waveforms are shown in Fig. 2 and Fig.3. Due to the injection phenomenon, the jitter of DPLL can be reduced.

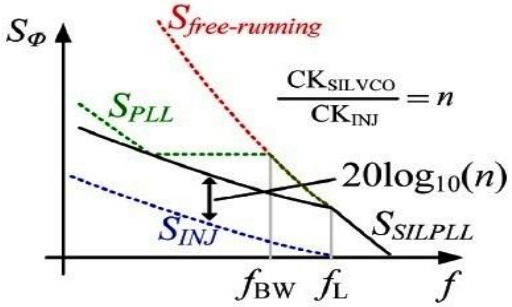


**Fig. 3: Output Phase Noise for SILPLL [8, 10]**

The proposed PLL consists of a third order PLL for 7.5 GHz clock generator and a first order DLL for self aligned injection. The third order PLL is composed by SILVCO, a divide by N frequency divider, a PFD, and an LPF. The illustrated output waveforms of the proposed DPLL with self aligned DLL are shown in Fig. 4.

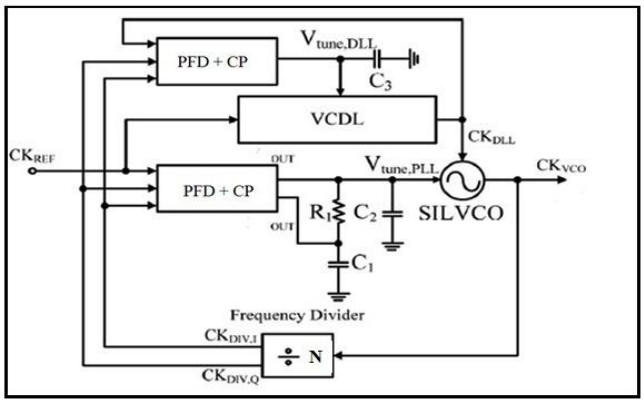


**Fig. 4: Block Diagram of Proposed 7.5 GHz DPLL with Self Aligned DLL [13, 14].**

The output phase and frequency are first locked to the input reference signal using the third order PLL, and then the injection phase for the sub harmonically injection locked VCO is automatically aligned using the first order DLL. In this proposed design, the loop bandwidth of the PLL is selected higher than the DLL. The phase and frequency of the sub harmonically injection locked VCO would be relocked to the reference signal again as the multiple frequency. The proposed self aligned method features excellent robustness, high speed, and simple circuitry.

To operate at a frequency N times higher, the loop bandwidth need to rise by factor N2. Hence VCO noise also increased. So loop bandwidth to be chosen one twentieth than reference frequency for stability of PLL. Here to suppress VCO noise DLL is added. This method is referred as injection locking [7, 8, 9, 10].

The first output phase or frequencies are locked to input reference signal using PLL. Then injected phase of sub harmonically injection locked VCO is automatically aligned using DLL. The oscillator locks to an external signal whose frequency is close to natural frequency. This phenomenon is known as “Injection Locking”. It is also possible for oscillator to lock at a frequency that integral sub multiple frequency of applied signal. Phase of PLL and VCO must align precisely to minimize Jitter. As VCO Frequency increases, Phase noise is also increases. To reduce jitter and phase noise, DLL can be introduced. Reference signal is also injected into SILVCO to further suppress the jitter. Improved PLL Locking reduces Jitter, phase noise and increases locking range [7, 8, 10].

The phase frequency detector is designed with Clocked Inverter and D Flip Flop using TSPC Logic as shown in Fig. 5. In this flip flop design only one transistor is being clocked by short pulse train which is known as True Single Phase Clocking flip flop.

The reset path of PFD is modified. The inputs signals data and dclock are directly connected to the reset signal of another D flip flop as shown in the Fig. 5. The reset path is eliminated; hence it reduces the dead zone.

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The circuit of D flip flop is also modified.
When clock and reset signals are low, node 1 will be connected to VDD through M2 and M5 devices. At rising edge of clock, node 2 will connect to ground through M6 and M7 devices. As node 1 is connected to VDD, turn off M3 keeping node 2 from charging high. Reset signal is charge up, node 1 is connected to ground through M5 and it pulls up node 2 due to switching M3 ON.
The job of M2 is to prevent short circuit between M1, M2 and M5. One inverter has been added at output because of getting flipped value of Q.

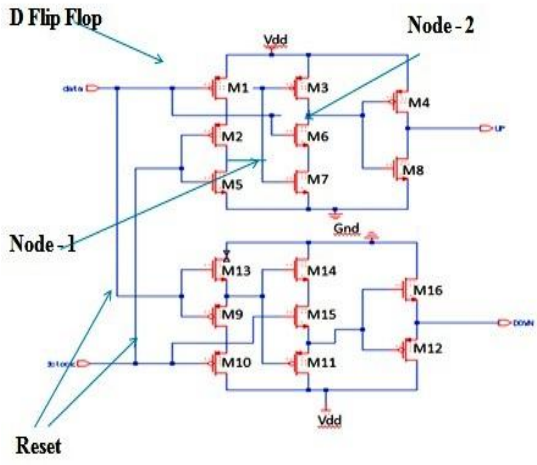


**Fig. 5: Schematic of Modified PFD**

The resultant waveforms of PFD are shown in bellow Fig.6. The measured power dissipation is 14.15 mW.

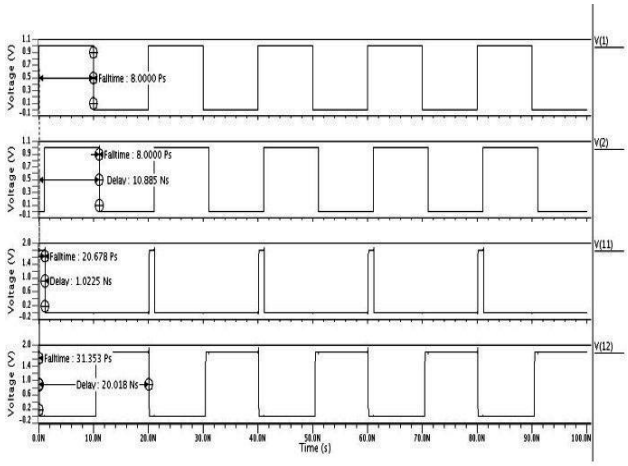


**Fig. 6: Output of Phase Frequency Detector at 50 MHz Data Leg**

The Charge pump is the next block to the phase frequency detector. As shown in Fig. 7, the output signals UP signal and DOWN signal generated by the PFD are directly connected to the charge pump.
It converts output of PFD digital signal into input of VCO analog signal either in form if voltage or current. Input voltage of VCO is formed by output of charge pump. The stability of VCO depends on charge pump, hence PLL becomes stable. Basically charge pump is formed by two current sources. Any mismatching of switches, current sources caused ripple on control voltage. It results in phase error as well as leakage current. Lower phase error means lower dead zone, lower mismatch and low noise. It should provide full swing so that clock will varies fully. One of the issues of charge pump design is leakage current. The phase offset and reference spur occurs due to presence of leakage current [2, 3].

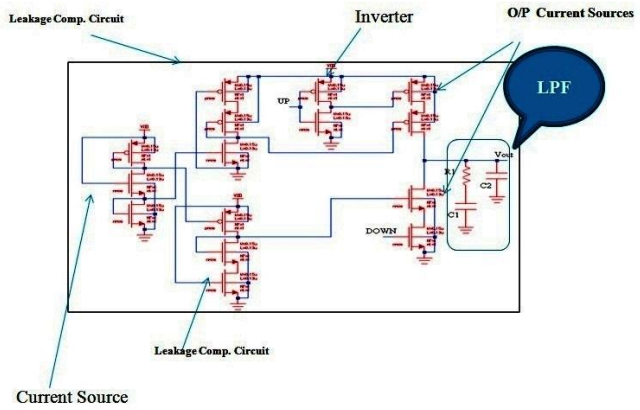


**Fig. 7: Schematic of Charge Pump with LPF**

The output response of the combination of PFD, CP and LPF is shown in Fig. 8. Normally power supply variations modulate the VCO output and due to which locking issues will be created. Here the current source is insensitive to voltage supply, so modulation of VCO can be minimized and hence leakage current is suppressed. To solve such issues, single ended differential charge pump design is used here. In this design charge pump circuit is composed using M18, M19, M23 and M28. Here leakage current I1 is almost equal to I2. Hence leakage current is eliminated using this concept. This circuit is also referred as leakage compensation circuit. M28 and M29 provides high output impedance, where M28 always put higher or equal in size than M29. Such charge pump design provides full swing, so clock can be fully varied [12].
The VCO design is shown in Fig. 9. Here, the coupling pair of M3 - M4 receives the single ended pulses at the gate of M4, and injects a corresponding current into the LC tank. The dimensions of M1 - M2 and M3 - M4 pairs as well as the bias circuit Ib1, M5, and Rb define the overall injection strength.

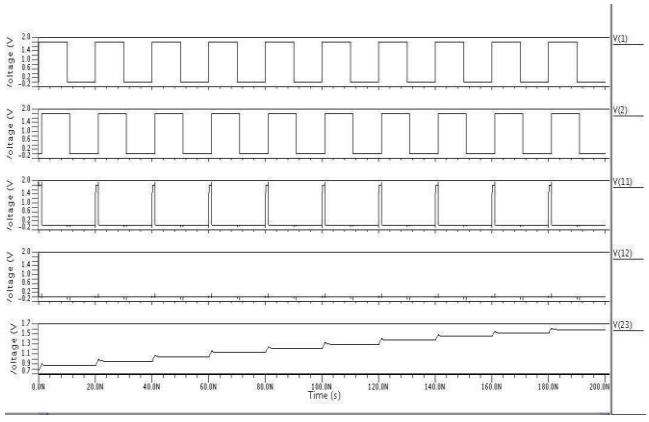


**Fig. 8: Combine Output Waveform of PFD, Charge Pump and LPF**

When nMOS switch is connected to differential node of VCO, the injected pulse becomes high. When the switch is turned ON and node is shorted. The pulse width should be less than rise/fall time of output for suitable injection.

The injection is achieved by connecting a differential pair to differential output of VCO. The odd harmonics are injected to VCO. Excitations of either M3 or M4 will decide odd or even harmonic injection. The other side is grounded [7, 8, 10].

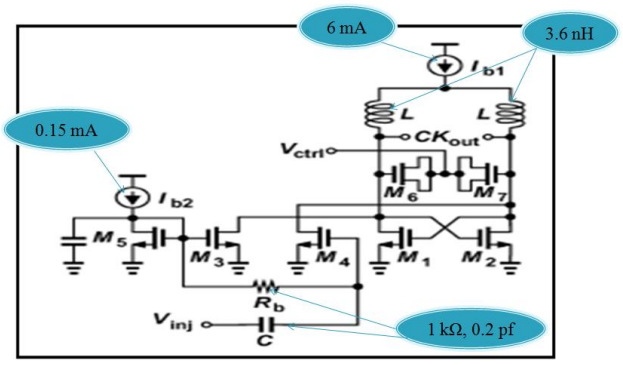


**Fig. 9: Schematic of SILVCO [8, 10]**

When the PLL is combined with DLL. The Harmonics of VCO is locked to the PLL. Hence the resultant output frequency is increased.

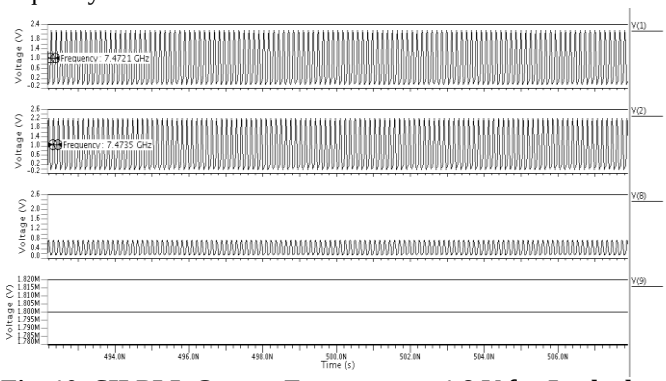


**Fig. 10: SILPLL Output Frequency at 1.8 V for Locked Response**

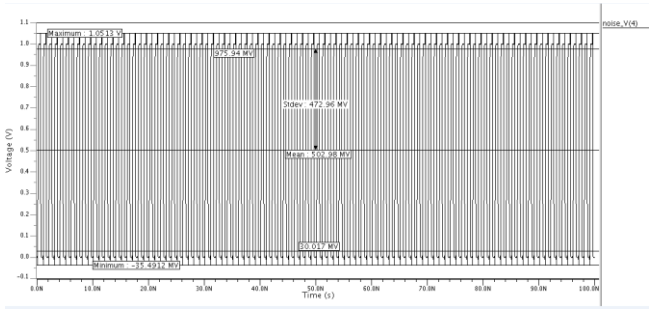


**Fig. 11: SILPLL Output Frequency at 1.8 V for Locked Response**

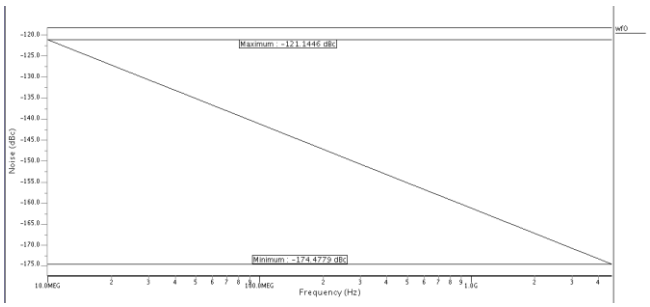


**Fig. 12: VCO Noise Measurement**

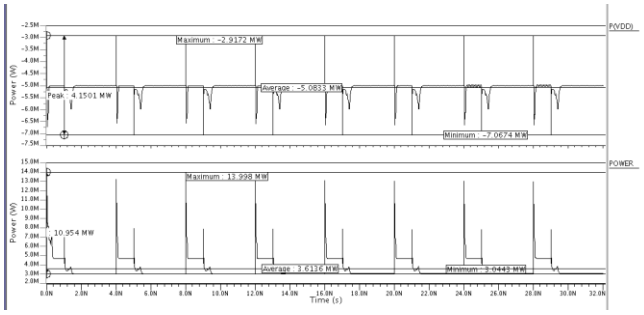


**Fig. 13: Power Measurement of VCO**

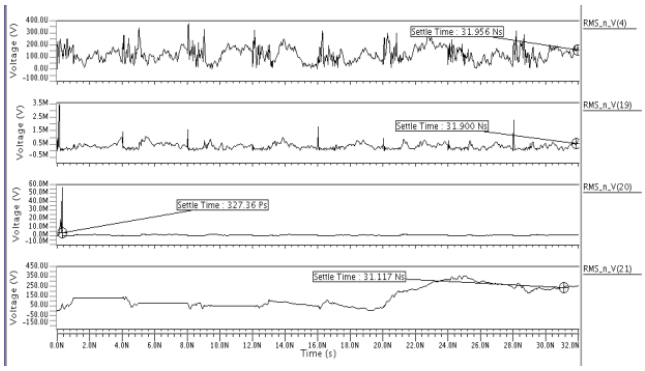


**Fig. 14: Deviation Measurement at Different Blocks (RMS Noise) (10 MHz – 10 GHz)**

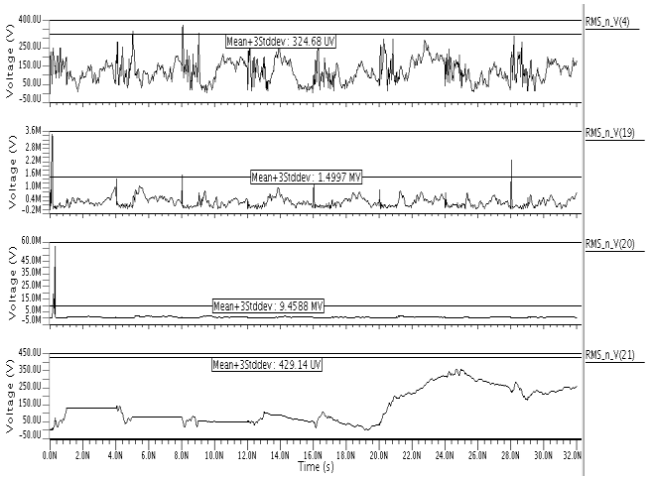


**Fig. 15: Settling Time Measurement at Different Blocks**

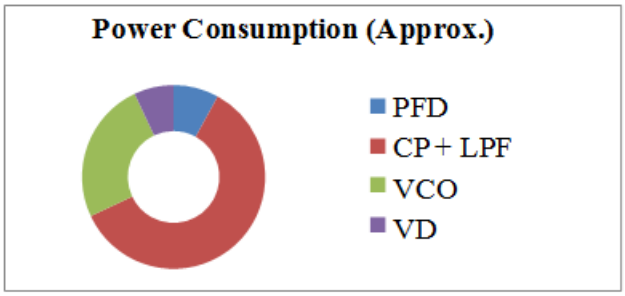


**Fig. 16: Power Consumption Chart**

Fig. 10 to Fig. 15 illustrates the measurement of various parameters of proposed Digital Phase Locked Loop. For each block of DPLL power dissipation is measured. The DPLL consume 7.8 mW and DLL consume 6.2 mW. The overall power dissipation is about 14 mW. The overall power consumption can be approximated for various blocks are given below in Fig 16 and Table 1.

**Table 1: Approx. Power Consumption**

| PLL Block | Power Consumption (Approx.) |
|---|---|
| PFD | 8% |
| CP + LPF | 55% |
| VCO | 30% |
| VD | 7% |

The phase noise analysis is also carried out at different stages as shown in mentioned results. It also concludes that the impact of phase noise is also optimum as compared to existing architectures. Proposed DPLL provide very wide tunning range. It can vary from approximately 7.25 GHz. It is very wide as compared to existing architectures. The settling time and locking range measurements are also carryout. Proposed PLL can lock within 15 cycles and also measured range is about 50 MHz. This result also shows that the stability of proposed PLL is also good as compared to existing architectures. Measured jitter noise is 110 fs after post layout results. This value is also very low by observing reported architectures.

## III. MONTE CARLO ANALYSIS

The Monte Carlo analysis is carried out for different blocks of proposed DPLL. The simulations are carried out using Tanner EDA. Total 500 iterations are taken for analysis. For PFD, dead zone analysis, for charge pump, maximum voltage swing and for VCO, output frequency analysis is performed. Fig. 17 to Fig. 20 shows the simulated results and output ranges of measured parameters at different blocks of proposed DPLL.

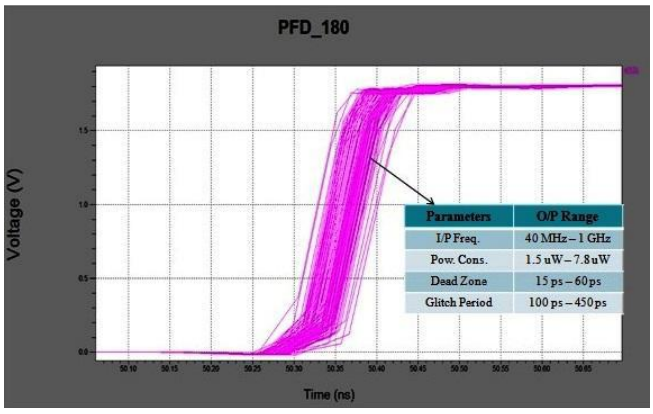


**Fig. 17: Monte Carlo Simulations of PFD**

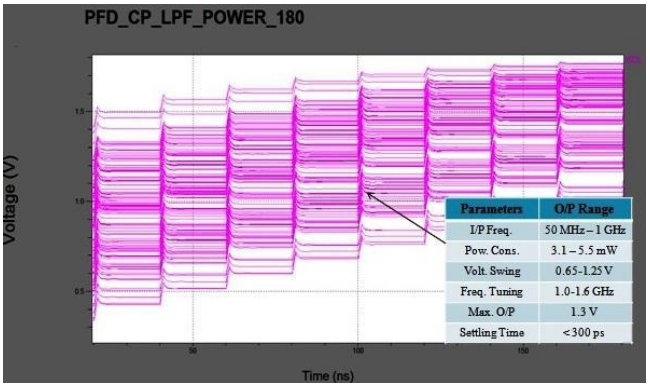


**Fig. 18: Monte Carlo Simulations of CP and LPF**

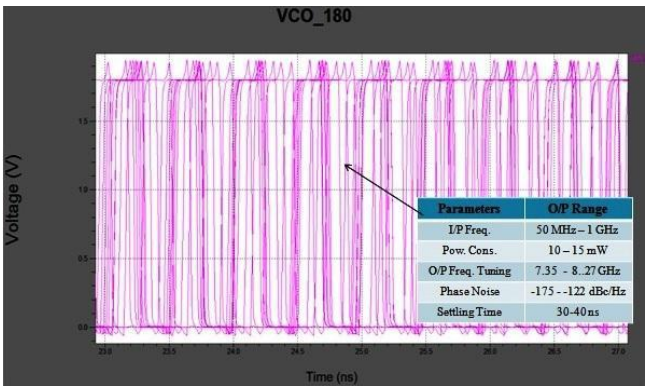


**Fig. 19: Monte Carlo Simulations of Proposed DPLL**

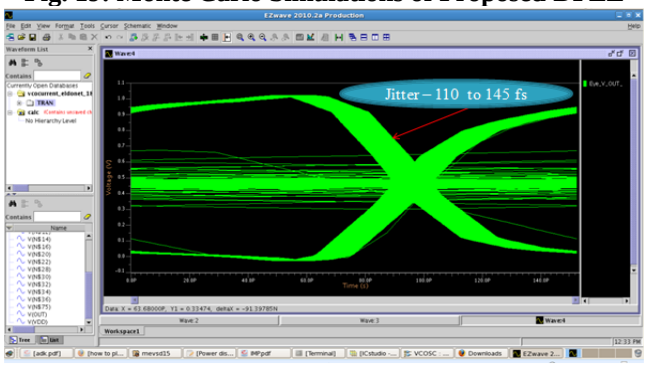


**Fig. 20: Eye Diagram of VCO for Jitter Measurements**

**Table 2: Performance Parameters of Proposed DPLL**

| Specifications | Proposed SILPLL Results |
|---|---|
| Technology | 180 nm |
| Supply Voltage | 1.8 V |
| Type of PLL | SILPLL |
| Output Frequency | 7.35 GHz |
| Ref. Frequency | 250 MHz |
| Frequency Tuning Range | 7.25 GHz - 8.1 GHz |
| Lock Range | 25 – 60 MHz (15 Cycles) |
| Settling Time | 31.12 nS |
| Integrated Jitter | 110 fs |
| Power Consumptions | 13.99 mW |
| Figure of Merit | -268.29 dB |
| Phase Noise at 1 MHz | -121.14 dBc/Hz |
| RMS AC / TRAN Noise | 30.27 V / 169.22uV |

## IV. CONCLUSION

To verify the proposed design the concept proposed the author used Tanner EDA and Mentor Graphics tools to carry out simulations in 180 nm CMOS technology. The proposed digital PLL have very stable high frequency signal output with wide tuning range. It is competent to generate high speed clock signal with minimum low phase noise and optimum power consumption. It is most suitable for the high speed ASIC applications.The proposed design is very low power with centre frequency of 7.5 GHz The measured phase noise of given PLL at 1 MHz reference offset frequency is -121.14 dBc/Hz with rms jitter is 110 fs for 7.47 GHz frequency.

Total dc power consumption is 14 mW. It gives very satisfactory circuit performance at higher frequency with minimum phase noise and jitter.

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## AUTHORS FROFILE

**Dr. Nilesh D. Patel,** He did his Ph. D. From Nirma University, Ahmedabad in VLSI Design area. He has obtained his M. Tech from Institute of Technology, Nirma University, Ahmedabad in 2008 in the field of VLSI Design. He did his B.E form SCET, Surat. He has published many technical papers in national and international journals. He has more than 18 years of experience in teaching UG & PG students. At present he is working as a Principal at M. L. Institute of Diploma Studies, Bhandu, Gujarat, India.

**Dr. Amisha P. Naik,** She is working as Associate professor at EC department, Nirma University, Ahmedabad since 2001. She teaches both at UG and PG level. She did B.E in Electronics from REC, Surat in the year 1997 and obtained M.Tech and Ph.D in VLSI Design area in the year 2006 and 2011 from Nirma University, Ahmedabad. She has published many papers in national and international journals. She is guiding three ph. d students in the area of analog and mixed signal circuit design.

**Dr. Priyesh P. Gandhi**, He presently works as a Principal at Sigma Institute of Engineering, Vadodara, Gujarat. He did his Ph.D and M. Tech from Nirma University, Ahmedabad with specialization in VLSI Design. His area of interest is Analog and Mixed Signal VLSI Design.