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Performance Analysis of Dual Edge Triggered Memory Cells using Multiple C-Elements

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Abstract: ***This research paper presents a low conditional discharge(C-element) Flip-Flops that are basic elements in all digital design. The existing circuits are power hunger due to the dynamic and static power dissipation increases. For reducing power consumption C element technique is used to reduce glitches at the data out. Results obtained through 130nm technology shows reduction in energy dissipation and delay. Average dynamic power dissipation of the proposed flip-flop is compare with two existing techniques. Average power of proposed flip-flop is reduced by 28.41% and 36.18% when compared with Latch-Mux flip-flop and Latch-Mux using C-element.***

Key Words: Dual Edge Triggering (DET), C-element, Latch-Mux, Flip-Flop.

I. INTRODUCTION

Flip-flops are basics storage elements used in many of Very Large Scale Integrated circuits, so they have to be designed with optimized power consumption. This paper presents the design of the Dual edge triggered (DET) flip-flops based on C-element using pass transistor technique. As the technology is scaling from micron technology to deep submicron technology the leakage power is one of the parameter which is effects the circuit performance. By using this technique the leakage power is reduced in the DET Flip-flops[1-6].

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The designs presented in this paper were simulated in CMOS 16nm technology using Tanner tool, observed to have superior characteristics such as power consumption and power-delay product (PDP) when compared to existing DET Flip-flops.Like Single edge triggered flipflop,also Dual edge triggered flipflop achieves the same data rate at half the clock frequency and leads to reduce power dissipation of synchronous logic circuits.Instead of using Single edge triggered flipflop,we can make possible for power savings by using dual edge triggered flipflop. A common Dual Edge Triggered (DET) flipflop design called Latch Mux DET flipflop and it has two input latches multiplexed to single output.A C-element is a three terminal device with two inputs and oneoutput[7],[9].When all the inputs of C-elements are same,the values of inputs and outputs are same,otherwise the previous output value is preserved. This device acts as a latch which can be reset and set with suitable combinations of signal levels at the input. New techniques of overlapping clocking schemes are analyzed in [11]. As nanotechnology is occupying equal space along with MOS technology nanometer devices for increasing clocking efficiency are presented in [12]. A Detailed scrutiny of various single edge triggered memory cells is studied in [13].

Low power very large scale integrated (VLSI) circuits have a great potential in the digital electronics.Dual-edge triggered (DET) flip-flops came into existence in the place of single edge triggered (SET) flip-flops[16-19]. As the DET flip-flops achieve the same data rate as of the SET flip-flops at half the clock frequency resulting in low power dissipation in the synchronous logic circuits. Latch-MUX DET flip-flop design is the basic design of the DET flip-flop, which consists of two latches at input where the latches are level-triggered by opposite clocks, Output of these latches are multiplexed to the final output stage through a multiplexer[20-23].

One of the latches is transparent to the output for every change at the output, In the presence of the glitches at the input the power consumption of the flip-flops will be greatly affected by these glitches. The Conditional toggle (CT_C) C-element flip-flop is one of the alternative DET flipflop design that can reduce the adverse effect of input glitches at the output. Leakage power is one the primitive to considered during the design of VLSI circuits in deep sub-micron technology; there are many techniques such as Dual sleep and Dual slack techniques forreduction of leakage power.

II.EXISTING WORKS

Simulations have been performed on three different DET flip-flop designs. The designs are:

1) Latch MUX DET design in [10]
2) Latch-MUX design, that uses a C-element at the output to perform the function of a MUX in [8]
3) Implicit-Pulsed DET flip-flop in [4]

Latch Mux Design:

Dual edge triggered flip flops usually consists of two latches and they are multiplexed to one output for proper operation. State of flip flop is changed by level triggering method. This result in a transparent latch following the changes that occurs in its input signal. It consumes more power and gives less performance. Here clocking activity results in more power dissipation when compared to transitions occurring in input signals. Circuit work here is based on selection of input clock signal. It involves transmission gate for transferring the value of D input to the output signal Q. It is similar to latch-mux single edge triggered flip flop. But they differ in arrangement of latches.

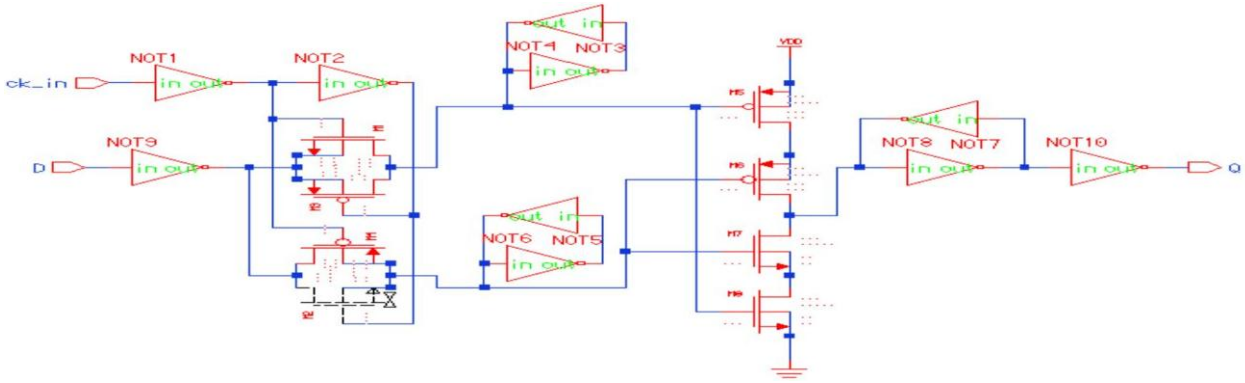

Fig.1 Latch Mux Flip flop

Latch Mux Design using C Element

The logic C element which is mainly used for capturing memory is used to perform the function of multiplexer in this design. Latches which are at higher and lower level receive input for operation. C-element shown in Fig: 2 acts as an inverter when both of its inputs are at same logic level. The weak structure used at the output has two functionalities. The C element's output is retained when PMOS and NMOS transistors are in an off condition. State of output is refreshed even in the presence of large amount of leakage current. Charge sharing issues that occur in circuit are eliminated by the back to back connected inverter circuit.

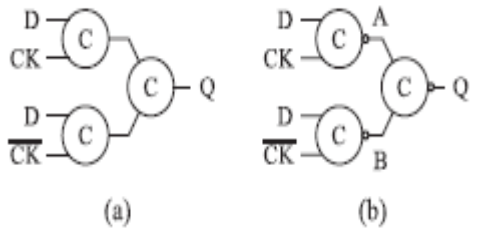

Fig: 2 Logic circuit of C-Element

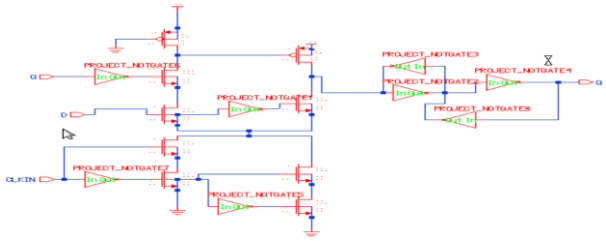

Fig.2 Latch Mux Flip flop using C-Element

III. PROPOSED WORK

Our proposed flip flop has 20 transistors and is having two data paths. The upper data path consists of a Single Edge Triggered flip-flop implemented using pass transistors. This works on positive edge. The lower data path consists of a negative edge triggered flip-flop implemented using pass transistors. When the input gets a positive clock pulse then the D input is transmitted in the upper data path and this one is constructed by using pass transistor logic. This operation is divided into two cases i.e., When the positive edge of the clock is applied to the circuit then the input is applied to both the paths but input data flows through upper data path through data transfer through few inverters and nmos transistors but any edge pulse ' l5' input is zero output 'Q' gets at output of ' l5' inverter.When the negative edge of clock is applied to the circuit then the input is applied to both the paths but input data flows through lower data path through data transfer through few inverters and nmos. In this case also input of ' l5 'is zero then output directly gets one but this operation is explained using idle case, in practical case we can get some power consumption appearing at output side due to the switching transactions and some leakage powers. In this method DET flip-flop consists of 20 transistors and also power consumption is little bit large compare to previous methods

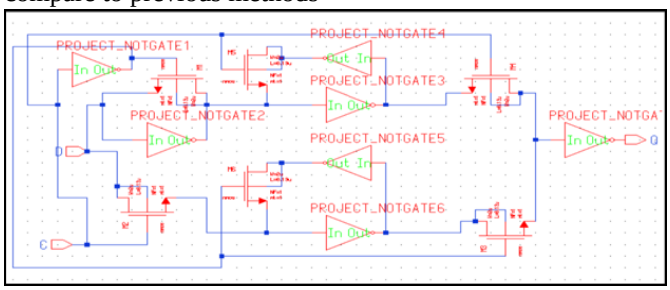

Fig.4 Proposed DET Flip Flop

IV. SIMULATION RESULTS

This section describes the performance of the proposed design using done using Mentor Graphics tool wave forms are shown for the proposed flip-flop in Fig: 4. From the output waveforms of fig:4 it is clear that the proposed Dual Edge Triggered flip-flop gives a glitch free output with minimum power dissipation and delay.

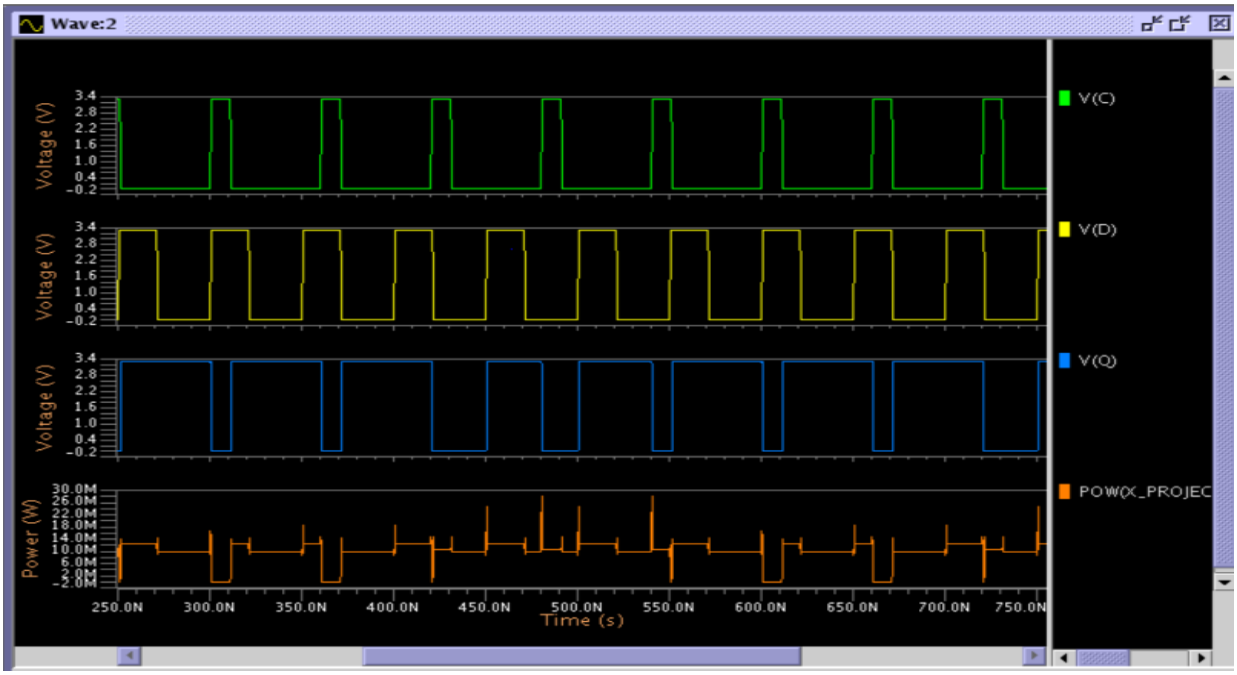

Fig: 4 Output Wave form of proposed technique showing glitch free output.

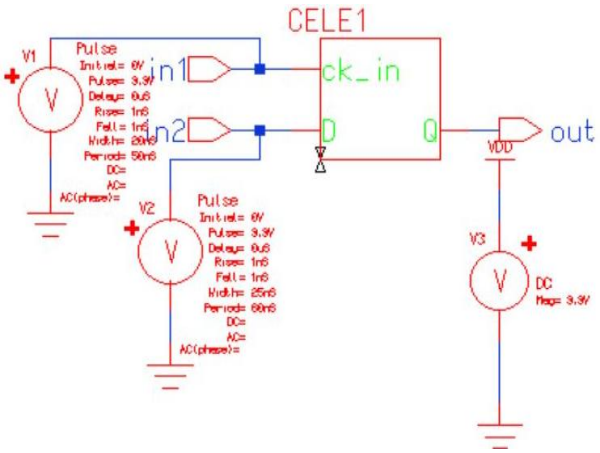

Fig: 5 Test Bench circuit of Latch Mux Flip flop using C-Element considered for simulation

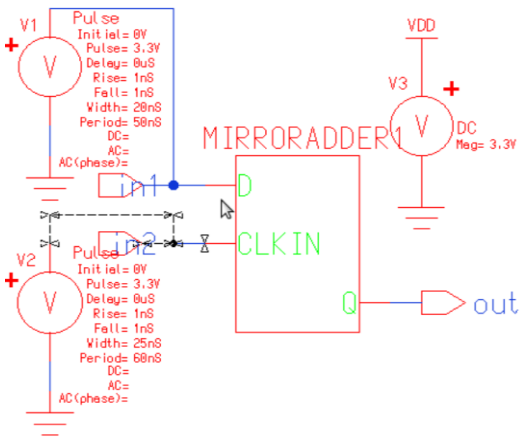

Fig: 6 Test Bench circuit of Latch Mux Flip flop considered for simulation

Table: 1 Power Dissipation Comparison of proposed and Existing Flip-Flops

Types of Flip-Flops	Various types of Power Dissipation Values			
	Maximum	Minimum	Average	Peak to Peak
proposed	26.468µW	87.540 nW	7.097 µW	24.46 µW
Latch-Mux DETFF	54.75 µW	90.09 nW	11.12 µW	54.47 µW
Latch-Mux using C-Element	32.264 µW	88.19 nW	9.914 µW	31.38 µW

From the above table:1 it is clear that proposed flip-flop shows very less values in all concerns of power dissipation. When comparing proposed technique with Latch-Mux Flip-flop in maximum and peak to peak power dissipation, but the average power dissipation has no much difference. Latch-Mux Flip-Flop using C-element shows less power values than Latch-Mux DETFF, but proposed technique is efficient than existing two techniques.

The following table:2 shows the delay analysis from table:2 we conclude that Latch Mux Flip-Flop using C-Element shows less delay when compared to proposed technique. This is due to fast switching structure of C-element.

Table:2 Delay Comparison of proposed with existing techniques

Types of Flip-Flops	Delay Types		
	Propagation Delay	Set-up Time	Hold Time
Proposed	1.41 nsec	12.17nsec	9.17nsec
Latch-Mux using C-Element	65.240 psec	32.05 psec	24.56 psec
Latch-Mux DETFF	26.3652 nsec	45.97 nsec	37.09 nsec

V.CONCLUSION

Two novel DET flip-flops have been discussed. The new proposed design is compared with existing circuits and we conclude that power dissipation and number of transistor count is improved. But the delay of the proposed circuit lies in between Latch-Mux with C-element and without C-element. The proposed circuit is also free from glitches which can be used for high performance scenarios. Voltage scaling performance can also be done to further study the performance to more logic depth.

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