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Design and Performance Evaluation of Ideal and Non-Ideal Effects of Pipeline ADC using Software Reference Models

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Abstract: ***Analog-to-digital converter (ADC) is one of the key component in any of the application oriented system design. This paper mainly focused on the simulation of various non-ideal parameters of an ADC as the number of resolution increases. The effect of non-ideal aspects like Jitter model and error block model are created in Matlab Simulink and the results are plotted. The dynamic non-ideal characteristics are discussed with their mathematical models and are compared with the equivalent resolution ADCs. The preliminary observations are also drawn according to the ideal characteristics. This shows that as the resolution increases, the bandwidth of non-ideal characteristics are also increases. This work is entitled to prove the non-idealities of 12-bit Pipeline ADC.***

Keywords: Pipeline ADC, Dynamic error, Harmonic distortion, SFDR, Gain error, Offset error, DNL and INL, Sample and Hold, Thermal noise.

I. INTRODUCTION

Analog to Digital converters (ADCs) which converts the analog data into digital information. ADC is one of the bridge between real world and digital world. The Architecture of ADC offers good tradeoff between high speed, power consumption and high resolutions. These parameters are required mainly for wide range of applications like digital audio and video, wireless communication information acquisition systems, measurement systems, data communication systems. Conjointly imaging and high accuracy instrumentation systems. The complexity in speed of conversion rate and high resolution of ADCs are become superior [3]. These ADC designs are modified to realize the product which reduces the time-to market. The speed of ADC and resolution will determine the performance of the whole system.

The design is for 12-bit resolution to convert digital to analog and analog to digital. The each step having an effect with clock jitter which will affect the signal accuracy [11]. The proposed work introduces the pipeline ADC model developed using MATLAB Simulink. In this work the different model has been introduced to evaluate the performance in non-ideal effects like sample and hold circuit, clock jitter and error blocks. These non-ideal building blocks are compared with ideal blocks of ADCs to verify the outcome [18].

ADC's and DAC play a very significant role in interfacing real time parameters with Digital processing systems. ADC's are integral part of DSP and communication systems. Pipeline ADC among different types exhibits better performance in terms of resolution. Conversion rate and power consumption are the parameters impact on the ADC performance at behavioral level. The non-ideal parameters of each block under behavioral model are characterized by the mathematical model. Behavioral model is suitable to study and analyze the non ideal conditions of ADC. Research studies have shown that different languages for behavioral modeling of various ADC's. This work analyses the non-linear behavioral effects of pipeline ADC using Matlab Simulink platform. This optimize the performs of real time constraints. The significant non-ideality parameters such as clock jitter, spurious free dynamic range, Total harmonic distortion, gain error, differential and integral non-linearity are modeled and Effective Number of bits (ENoB) are estimated and analyzed to map the effects on the performance of Pipeline ADC's.

II. DYNAMIC NON-IDEALITIES

In this section, high priority is considered as one of the point in dynamic non-ideal parameters [2] of Pipeline ADC. The proposed work is compared with an existing research for the non-ideal parameters to prove the better results with various types of ADCs [2]. ADC behavioral performance has a direct impact by non-ideal conditions of real time parameters. Non-ideal parameters for ADC are categorized into two subclasses static and dynamics. Some of the dynamic non-ideal parameters of ADC have great impact on the performance and taken in this study are offset error, gain error diffusion and non-linearity error [20].

A. Total Harmonic Distortion (THD)

In an ideal case the input signals are considered such that phase frequency and amplitude are determined. For the total harmonic distribution the input frequency of a variable is defined to convert the input to get pure amplitude [17].

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$$S_{out,\ THD}(t) = S_{in}(t)|f = f_{sig} + \sum_{i=2}^{p} HD_i S_{in}(t)|f_i = if_{sig} \quad (1)$$

In which $S_{out,THD}$ denotes the output after the THD step.

B. Spurious Free Dynamic Range (SFDR)

Generation of Spur's frequency and applying the relevant amplitude in a harmonic to model the SFDR parameter. Thus, the output of this stage can be written as follows:

$$S_{out,\ SFDR}(t) = S_{out,\ THD}(t) + SFDRS_{in}(t)|f = if_{sig} \quad (2)$$

C. Offset Error

Offset values are added to the output of SFDR to generate the offset error. This will affect the output according to the offset error's definition. The output after this stage can be expressed as follows:

$$S_{out,\ off}(t) = S_{out,\ SFDR}(t) + \delta \quad (3)$$

D. Gain Error

Pure amplitude should be multiplied with the gain error and added with the previous signal to model the gain error effects. The output after this stage can be expressed as follows:

$$S_{out,\ G}(t) = S_{out,\ off}(t) + \eta_G S_{out,\ off}(t) \quad (4)$$

E. Differential Non-Linearity Error (DNLE) and Integral Non-Linearity Error (INLE)

The aim of INL and DNL modeling is to change the transition code length moves the ideal transfer function [4]. The mean value is for INL and the range of uniformly random source is for DNL. Parameters and variables should be defined for end user. The general random source to be added is:

$$\text{Stable}\left\{\left(\frac{\text{INL}-\text{DNL}}{(2^n)-1} \times V_{FS}\right) : \left(\frac{\text{INL}+\text{DNL}}{(2^n)-1} \times V_{FS}\right)\right\} \quad (5)$$

A different method can be presented but, this shows the internal structure of the ADC. A third order power series is used to model the INL and DNL, the input Γ_{in}.

$$\Gamma_{out} = \Gamma_{in} + \mu_1\Gamma_{in}^2 + \mu_2\Gamma_{in}^3 \quad (6)$$

With respect to INL and DNL two peaks negative and positive values of a signal is restricted. The range from maximum positive and minimum negative values cannot offered by producing a method which can completely modeled. The output can be modeled after the first stage as:

$$S_{out,(D\,\&\,I)NL}(t) = S_{out,G}(t) + \varrho|\text{Stable}\{\alpha:\beta\} \quad (7)$$

First method is shown, and:

$$S_{out,\ (D\,\&\,I)NL}(t) = S_{out,G}(t) + \Gamma_{out}|\Gamma_{in} = S_{out,G(t)} \quad (8)$$

III. BEHAVIORAL MODELING OF PIPELINE ADC

A. Architecture of Pipeline ADC

The architecture of Pipeline ADC is shown in fig. 1. Pipelined ADC proposes superior trade-off involving speed of conversion rate, power consumption and resolution of bits. It consists of 12-bit cascade stages, timing circuits, digital encoding and correction block. This architecture is suitable for high speed conversion rates. On simultaneous operation is carried out at every stage. The entire speed of this architecture is totally dependent on the first stage.

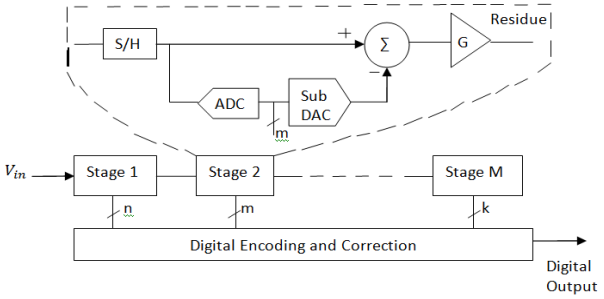

Fig. 1. Architecture of Pipelined ADC

The general block diagram of pipeline ADC consists of M stages and sample and hold circuit as shown in figure. The internal structure of each pipeline stage M consists of four sub-blocks, a sub-ADC, with $N_i < 2^{ni}$ output codes a sub-DAC, an adder and a sample and hold residue amplifier. All these sub-blocks are implemented as a single MDAC [15].

B. Sample and Hold Circuit

The sample and hold circuit samples the amplitude of input signal and then holds the constant voltage level until the next sample is acquired. Sample and hold plays a significant role in ADC as the input signal is exists for sufficient time to complete conversion of analog to digital. The sample and hold circuit is shown in the fig. 2.

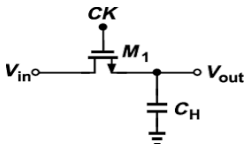

Fig. 2. Typical representation of sample and hold circuit

When switch is closed by the clock, the sampling capacitor is charged by input signal. This process is called sample and also known as track. Once the switch is open the sampling capacitor voltage is kept in the instantaneous value, and is referred as hold. This process is called hold [19].

The voltage transfer function, bandwidth and sample and hold circuit meet the condition:

$$H(j\omega)| = \left|\frac{1}{j\omega R_S C_H + 1}\right| \quad (9)$$

$$BW = \frac{1}{R_S C_H} \quad (10)$$

The sample and hold circuit is modeled by considering the non-idealities of offset errors. The thermal noise is one of the main noise for high speed sample and hold circuit. The noise density is:

$$v_n^2 = 4KTR_s \tag{11}$$

Combination of the transfer function (9), the output noise is:

$$\overline{V_0^2} = \int_0^\infty V_n^2 \,|H(j\omega)|df = 4kTR_s \int_0^\infty \frac{1}{1+(2\pi f R_s C_H)^2} df = \frac{kT}{C_s} \tag{12}$$

In order to decrease the noise impact, to increase the C_H, but the expression (10) shows that the increasing of sample capacitance will leads to a time limit in bandwidth. To ensure the bandwidth increase the size of switch transistor this reduces the conduction resistance [1].

C. Sample and Hold Block Simulink

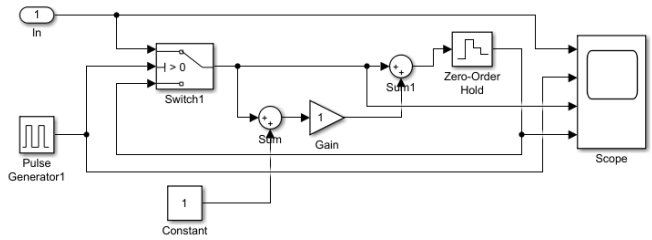

Fig. 3. Sample and hold block model

Fig. 3 shows the SIMULINK model of the sample and hold circuit. It is constituted of several blocks each of them composed by sine wave, pulse generator, constant, switch, gain, zero-order hold and analog output. The error is occurred in sample and hold circuit when the input voltage is zero and the output voltage is nonzero value. This offset error voltage exist in both the sample and hold time during the hold process, sample and hold circuit holds the last value of the sample. This modeled offset error is added to the constant value in every sample and hold phase. In frequency representation, zero order hold function is equivalent to multiplication of signal spectrum by a sinc function. The output at various stages of sample and hold circuit is shown in the fig. 4.

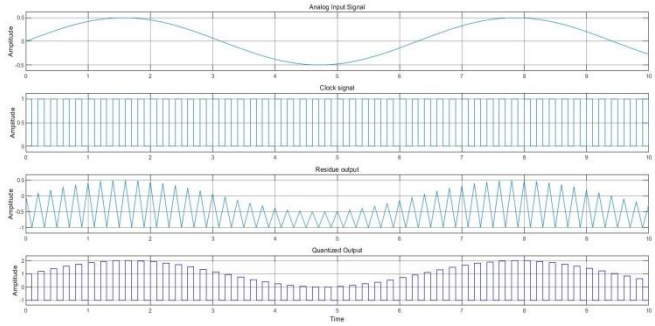

Fig. 4. Output characteristics of sample and hold circuit

D. Clock Jitter Model

Clock jitter is defined as the abrupt variation in sampling time due to phase noise of the clock generator and also by the sampling. The clock jitter is assumed to be white noise with uniform distance between the range from 0 to $f_s/2$ where f_s is the sampling frequency.

Mathematically the clock jitter of a sampled signal is given by

$$S_i'(t) = S_i(t) + \delta \times [S_i(t+1) - S_i(t)] \times f_s \tag{13}$$

δ is the deviation in sampling time, $S_i'(t)$ is resultant error due to clock jitter with f_s as the sampling time. Using Taylor's series expression (13) can be expanded as

$$\delta \times [S_i(t+1) - S_i(t)] f_s \approx \delta \times \frac{d}{dt} S_i(t) \tag{14}$$

The effect of clock jitter leads to non-uniform sequence of samples [4]. This increases the error at the Power spectral density of pipeline ADC as shown in fig. 5.

The modeling clock jitter using MATLAB Simulink is as follows. The input signal frequency $S(t)$ with amplitude A and frequency f is sampled at instants 'δ' is expressed as [16]

$$S(t+\delta) - S(t) \approx 2\pi \times f_{in} \times \delta \times A \times \cos(2\pi f_{in} t) = \delta \times \frac{ds(t)}{dt} \tag{15}$$

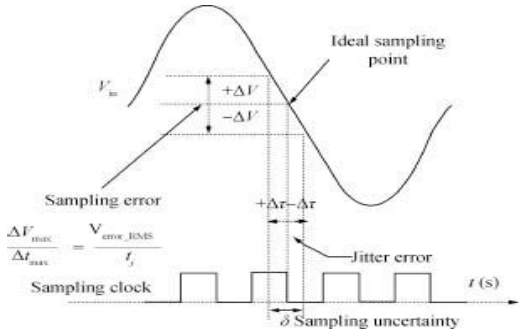

Fig. 5. Error of Clock Jitter

The sampling instant deviation δ is introduced into the modeling by a Gaussian random process with standard deviation $\Delta\tau$. The clock jitter model is shown in the fig. 6.

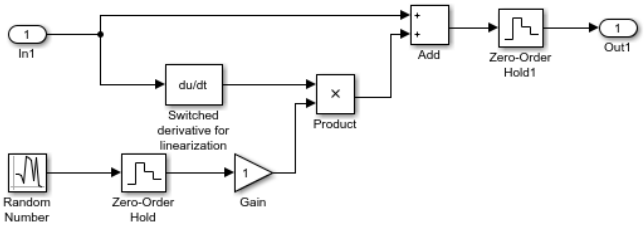

Fig. 6. Simulink model of Clock Jitter block

The Clock Jitter block model is shown in fig. 6. It consists of random number, switched derivative for linearization, zero-order hold, and gain. Normal distributed random numbers are generated by the Random number block. This Gaussian noise is used with sampling time to hold the mean coherent with the gain block. Constant input is sent to the switched derivative with proper transfer function approximation for linearization of both the outputs. These outputs are scalar and specify the number of input ports to be multiplied. To emphasize the jitter effects, sample the input signal at the clock frequency. This indicates if the clock is jitter free, use the same sample only.

When the jitter is added to the clock by random Gaussian number as a delay, the sampling output is presented as noise is proportional to the jitter value with the variation of the input signal.

Using a finite sampled input signal the number of states in the sinusoidal input is also finite. An output characteristic of clock jitter is shown fig. 7.

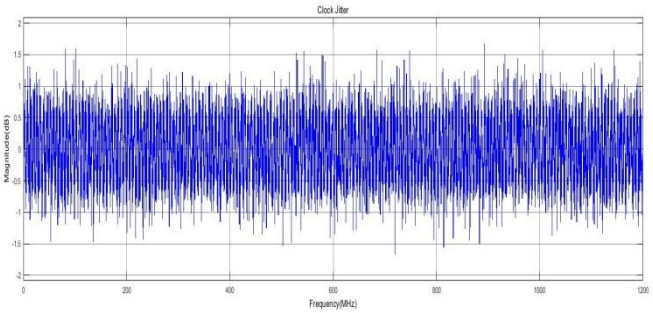

Fig. 7. Simulated clock jitter characteristics for ADC

E. Error Block Model

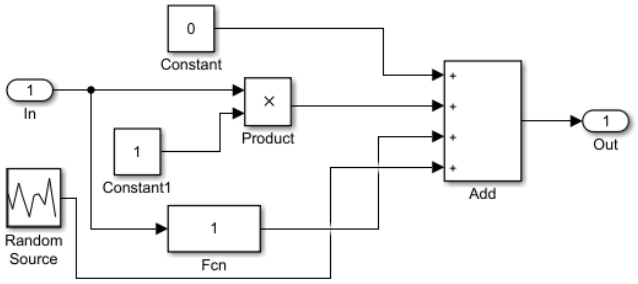

Fig. 8. Error block model

The error block model is shown in figure 8. It represents all kinds of errors can modify the input sine wave parameters before the conversion process. These errors are the result of imperfections of the manufacturing process. The effect of error is usually a constant near to zero. The gain is a multiplicative error which is commonly assumed constant. The non-linearity block is modeled by a polynomial function. The last modeled error is always added to the model as a random Gaussian noise. The plot indicates the output characteristics of error block as shown in fig. 9.

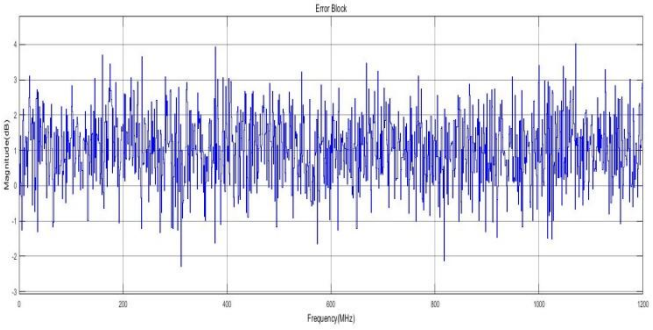

Fig. 9. Output characteristics of Error block

F. Time Interleaved ADC Model

The method of time-interleaving ADC model consists of placing a Multiplying ADC with duty cycle interleaved between them. The ADCs are accumulating to convert the equivalent signal. Once the conversion operation takes place, each and every output signals are multiplexed. The fast conversion operation takes place in this architecture, for the number of parallel ADCs in the circuit conversion rates are determined.

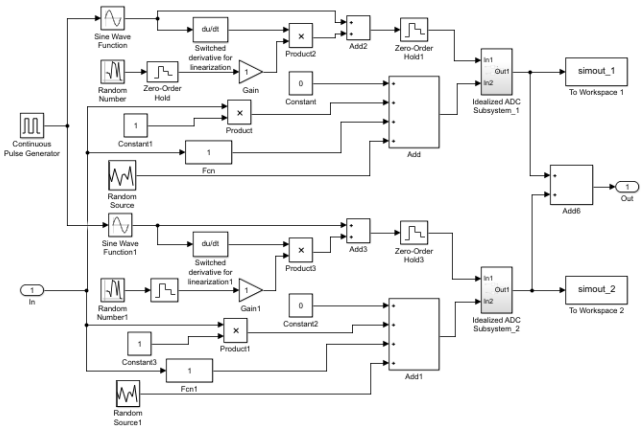

Fig. 10. Time interleaved ADC model

At high conversion rate functions, such as dual channel digital oscilloscope and time-interleaving ADC method is an attractive selection. This method is used in two conditions; when the function involves a high conversion rate but not accomplished by a single ADC; or when the manufacturing cost is reduced using lower cost parallel ADC than a high conversion ADC.

The time interleaved ADC model developed in Simulink is shown in fig. 10. The ADC resolution of 12-bits, error model and clock jitter model are created. The plot is obtained by creating many subsystems as shown in fig. 11.

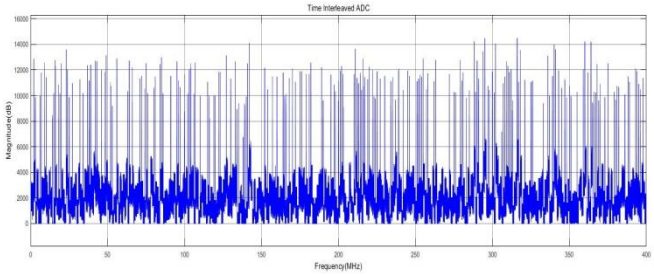

Fig. 11. Output characteristics of Time interleaved ADC

IV. POWER SPECTRAL DENSITY

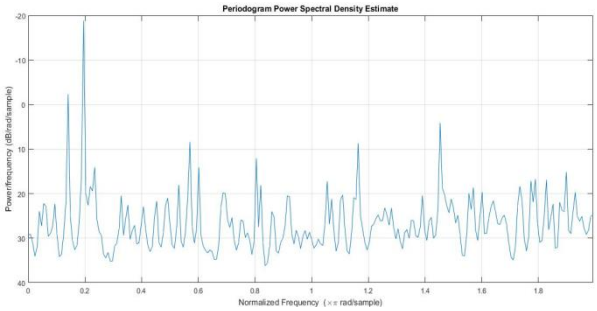

Fig. 12. Power Spectral Density

The output of the converter amplifier and ideal quantization with jitter is observed. From the observation, it is noticed that the jitter effect increases the noise effect which results in decrease in the Signal to Noise ratio (SNR).

This SNR is calculated with the jitter contribution about 55.8dB and it is less than the ideal maximum value.

V. RESULTS AND DISCUSSION

Table- I: Effect of offset errors

Offset (v)	SNDR (dB)	SFDR (dB)	ENoB (bit)
0	74	102.8	12
0.0012	72.654	92.4	11.78
0.1	55.8	71.6	8.04

The table –I summarizes the parameters like SNDR, SFDR and ENoB form the above experiment. This predicts that the variation in the offset voltage results in the proportional changes in respective parameters. At zero offset voltage ENoB will reach at 12-bits resolution and the same ENoB reduce to 8-bits, when the offset voltage is increased to 0.1v. From this, it is evident that as the offset voltage increases which reduces the resolution of a converter.

VI. CONCLUSION

This paper summarizes the various non-ideal characteristics of ADC under dynamic category. The high resolution is greatly affected by number of non-ideal parameters like SFDR, gain error, INL, DNL and offset error. To analyze the error rate, jitter model and error blocks are modeled through Simulink. Sample and hold circuit is modeled using Simulink to feed the input for other non-ideal blocks. These error blocks output is plotted and estimated the peaks for noise interpretation. Here SNDR, SFDR, and ENOB are calculated for the various offset voltages and respective effects are analyzed. It shown that increased noise rate at the input level greatly affect the ENOB and SFDR even has the high resolution for widest range of computation. An overall finding from the simulation gives error impact on resolution.

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