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Design of a Floating Gate Synapse Simulation Model

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Abstract: ***Proposing a simulation model of Floating-gate (FG) MOSFET whose characteristics when operated at sub-threshold conduction are like a synapse of brain. It can store, program, and adapt information (charge). The model consists of empirical equations and its parameter values have been extracted from fabricated results. The post fabrication programming of charge at the FG have been observed using two quantum-controlled processes (Fowler Northeim tunneling & hot electron injection) with the help of externally applied voltages, which in turn program FGMOS characteristics like threshold voltage, V_{th}. The programming is non-volatile and stable with changing temperature (4μV/°C) and noise. The V_{th} programming range is varied by more than 7V to 8V of its original value with very high bit (about 13-bit) of programming precision/resolution. The model layout/mask consume maximum of 130×90 μm^2 of chip area and average power consumed by model is around 0.315mW. This verified FG simulation model can introduce the concept of on-chip tuning ability, programming ability, reconfiguring ability in precision analog signal processing designs like inductor, filters, controller circuits, voltage-controlled oscillators, etc. On adding adequate feedback mechanism to FGMOS model, it shows self-adaption of FG charge, which can be used to emulate features of a neuron/synapse in CMOS based neuromorphic circuits emulating several cognitive behaviors of human brain like Winner takes all circuits, circuits generating spikes (STDP), etc.***

Keywords: ***Fowler-Northeim Tunneling, Neuron, Injection, Non-conventional MOSFETs, Synapse, Post-fabrication programming.***

I. INTRODUCTION

Analog circuit based on CMOS technology is needed more than ever like high definition TV, cardiac monitoring devices (EEG, ECG) require precision analog signal processing units to detect small signals buried in noise. Satellite or Radar communication require RF transmitters and receivers, automobile industry require micro electro mechanical systems like accelerometer, gyroscope etc. [1-3]. Modern mobile devices require analog power management unit for prolonged battery life.

There is also an emerging trend of neuromorphic engineering in which cognitive behavior (continuous learning, self-adaption, vast memory) of human brain have been simulated using CMOS based circuits, like bio-inspired CMOS vision chip, CMOS amplifier, neural CMOS IC and their application to data classification[4,5]. An analog CMOS cellular neural network for biologically-inspired walking robot and bio-inspired optical flow circuits has also been developed [6-8]. CMOS designs are advantageous in terms of compactness, power consumption and precision.

Still less preferred as compared to digital designs (processing units), because of few design challenges. Analog design cycle requires several iterative steps to optimize the sizing and biasing condition of the circuit.

Always a tradeoff between design time and design accuracy has to be maintained. With process variations (offsets) accurate prototyping of a design is very difficult and time consuming. Analog technology lacks in reconfiguring ability/on-chip programming ability. Several efforts have been made to overcome these shortcomings. Special layout techniques, calibration schemes, laser trimming circuitry, digital tuning circuitry have been introduced in analog designs [9-12]. Field programmable analog array introduces the concept of rapid prototyping [13, 14]. However, all these solutions require huge circuitry or large switching circuits, which in turn reduce compactness and increases power consumption. The need is to discover solution within analog domain which leads the technology towards development of non-conventional MOSFETs. With the use of different materials like high-k gate dielectric, metal gate electrodes, materials other than Si like In GaAs, carbon, etc., different processes (strained Si, etc.) and different structure (silicon on insulator), non-conventional MOSFETs have been developed. SOI based double gate FET, FinFET or multiple gate FET introduces programming ability in analog domain [15, 16]. The short channel effects due to scaling down of conventional MOSFETs increases their demand but they use special costly fabrication techniques. Proceeding towards state of the art we are proposing a floating gate technology based Floating gate MOSFETs. The FGMOS are just like conventional MOSFET with an additional gate called FG, which is covered all sides by oxide. The charge once introduces at the FG remain trap for years. The charge can only be programmed using quantum processes (Fowler Nordheim tunneling and hot electron injection). Recently several FG technology based simulation models have been developed [17-20]. The future work in FG technology is to develop FG synapse model at lower technology so that circuits can work at higher frequency. However scaling down brings various challenges.

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There are papers presenting scale down simulation models of FG transistors [19]. Thus, with the previous knowledge and usability of FG technology the work shown in this paper is distributed in following sections: first section deals with FGMOS double poly-structure and final mask sent for foundry. Later section deals with the characteristics of fabricated FGMOS transistors and its threshold voltage programming. Using hardware results FGMOS simulation model have been verified. The model is flexible and can be used at wide operating frequency range, thus can be used to introduce on-chip tuning ability, programming ability in RF to low frequency analog signal processing devices [21, 22]. Using a capacitive feedback in the FGMOS structure, the change in FG feedback through capacitor to increase injection under continuous tunneling which in turn, self adapt this change of charge at FG. Self-adaption feature of FGMOS is used to emulate a synapse/neuron of human brain, thus used in several neuromorphic circuits [23-25].

II. FLOATING GATE MOSFETS

A. FGMOS structure

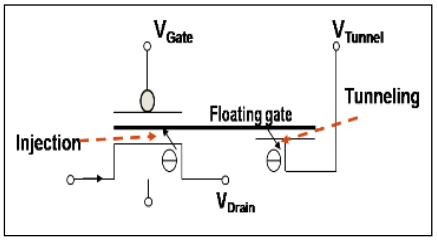
FGMOS are just like conventional MOSFET with an additional gate called FG, fabricated using double poly structure (poly 1 used for FG and poly2 for control gate). The FG is electrically isolated and covered all sides with oxide. The charge once introduce at FG will remain trap for years. Thus, FG transistors have been used as storage element (EEPROM, flash memory), where programming of charge is not performed in controlled manner. The charge at the FG can be programmed precisely using two quantum processes, Fowler Nordheim Tunneling and Hot electron injection. Figure 1(a) depict symbolic representation of injection and tunneling mechanism at the FG PMOS where FG is electrically isolated and double poly structure making input capacitor (of value 250fF) distinguishes FG from control gate (used as conventional gate of FGPMOS). A junction is created, connected with FG through a MOS capacitor (V_{Tun}), called tunneling junction. Figure 1(b) illustrates structure of FGPMOS where biasing topology used for tunneling and injection of charge is also depicted.

B. FGMOS programming techniques

In Fowler Nordheim tunneling a high positive potential is applied at the tunneling junction. High electric field between tunneling junction and FG causes charge (hot e) to tunnel out from FG. Thus, negative charge reduces at the FG and threshold voltage increases, as shown in I_d-V_{gs} plot of FGNMOS in Figure 1(c). In hot e injection with high electric field between drain and channel (source), charge carriers of channel get energies, hit the substrate atom, impact ionization takes place, and avalanche of e-hole pairs generation occur which in turn energies the carriers, hot electrons gain enough kinetic energy to cross Si-SiO_2 barrier and through oxide inject at the FG. Injection increases the negative charge thus reduces the positive threshold voltage of FGNMOS, shown in Figure 1(c). Similar changes in I_d-V_{gs} plot with tunneling and injection can be observed in the case of FGPMOS. PMOS shows better injection of charge as compared to NMOS (holes generate e-hole pairs and hot electrons crosses the barrier and inject to the FG) [26]. To program FGNMOS a programmer PMOS is used for injection at common FG, illustrated in Figure 1(d). Thus, Injection can be either performed directly (using V_{ds} of respective FGMOS) or indirectly (using programmer PMOS at common FG). In indirect type of programming, FGMOS need not to be removed from circuit for its programming. In papers [26, 27] it has been claimed from experimentally verified results that with tunneling/injection mechanism $V_{th}$of FGMOS can be programmed by about 13 to 14 bit of programming resolution.

C. Fabricated FGMOSs

The FGMOS designs mask is generated using Cadence Virtuoso considering design layers specified from foundry (directly programmable FGPMOS layout and complete 40pin Mask is illustrated in Figure 2(a) and (b)). The three of its design are fabricated using On Semiconductor C5 AMI process from MOSIS fabrication services USA, packaged in form of 40pinDIP IC. (Shown in Figure 2(c)) The IC is being first tested and then to characterize FG transistors Keithley 4200 Semiconductor Characterization System is used. The system can interface software with hardware using SMUs (source measuring units). A four terminal project has been developed in system software (KITE) and with the help of four SMUs current/voltages are sourced as well as measured at the four terminals of the device. The four terminals of FGPMOS are drain, source, gate and tunneling junction (substrate and source is internally shorted) and are connected with the system through a four terminal fixture and four SMUs. Testing set up is demonstrated in Figure 2(d), consists of SCS machine, PIV 1800 test fixture to test four terminal devices, breadboard, and fabricated ICs and connecting wire.



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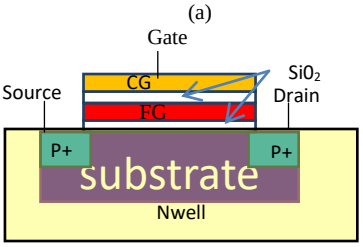

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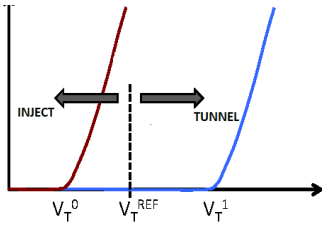

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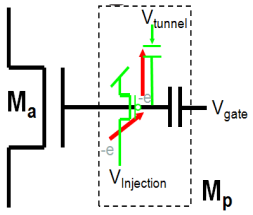


(d)

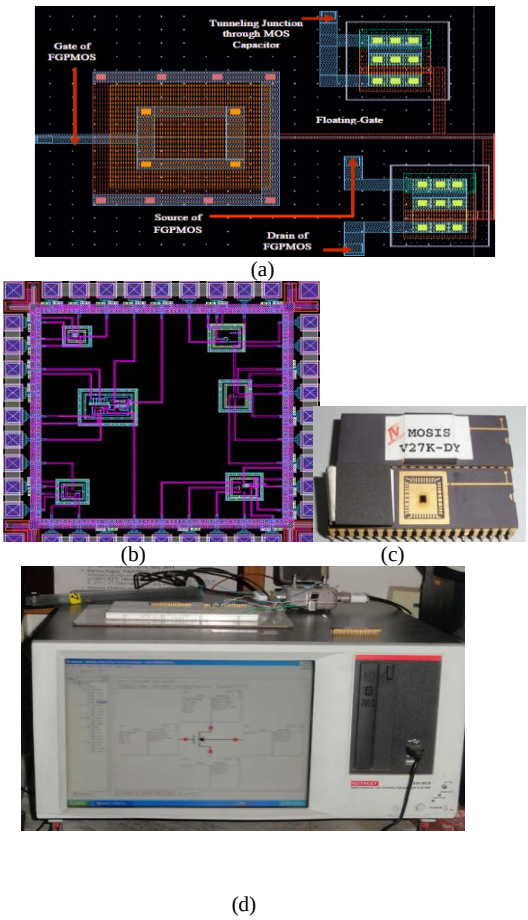
Fig.1 (A): Symbolic Representation Of Fg Charge Programming In Fgpmos (B): Fg Pmos Structure (C): I_d-V_{gs} Plot Of Fgnmos (D): Indirectly Programmable Fgnmos Using A Programmer Pmos At Common Fg.

III. HARDWARE TEST RESULTS

The testing of FG transistor and on-chip programming is being performed in following steps. First initial operating condition of the transistor is observed (I_d-V_{ds} and I_d-V_{gs} characterization plots). Corresponding to the initial threshold voltage V_{th}, on-chip programming range, corner values of tunnelling and injection voltages and programming precision has been estimated. When both processes are operated simultaneously an equilibrium condition is achieved and charge at the FG gets stable after effects of both processes nullify each other. Such equilibrium operating conditions have also been estimated. Three of the FGMOS transistors have been fabricated in IC are tested one by one in all five copies of IC.

A. Directly programmable FGPMOS

Using SMU respective drain, source gate voltages are sourced and I/V are measured using system. According to the pin configuration of design in IC respective SMUs are connected. Characterizing plots I_d-V_{ds} at different gate voltages and I_d-V_{gs} have been observed (Figure 3(a) and (b)). It shows unwanted initial condition due to process variation as value of V_{th} is equal to +1V.

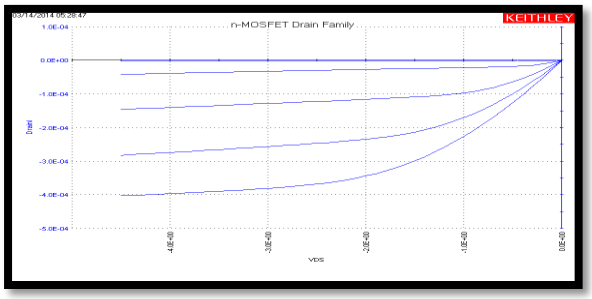


(a) (b) (c) (d)

Fig.2. (a): Layout of directly programmable FGPMOS (b): Complete mask of IC (c): fabricated 40pin IC (d) Keithley 4200 SCS testing set-up.

B. Tunneling

A high positive voltage (V_{Tun}) is sourced at the tunnelling junction using forth SMU for tunnelling. Initial value of V_{th} is 1V thus to correct the offset tunnelling is performed first. The tunnelling voltage V_{Tun} is sourced with values between 10V to 12V. Tunnelling starts beyond 10.75V and change in V_{th} is from +1V to +0.5V. Then V_{Tun} is sourced with voltage 12 to 13 V in 5 steps (step size of 0.25), the value of V_{th} gets programmed from +0.5V to -2V, illustrated in Figure 4(a). After removing V_{Tun} at relaxed state when characteristic is measured, the value of V_{th} becomes equal to -1.5V (shown in Figure 4(b). After tunnelling till 13V in 8 successive steps and due to internal injection effect, this change of 0.5V in the value of threshold voltage is observed. Equilibrium between two processes is achieved and a fixed value of charge at the FG and hence, V_{th} is achieved.



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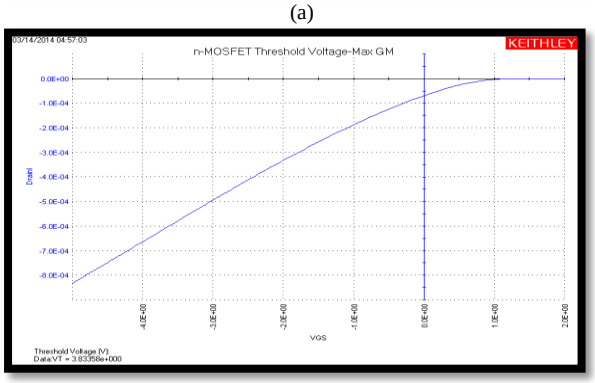
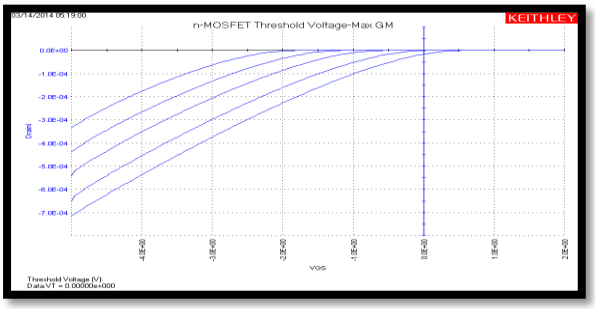


(b)

Fig.3. (a): Id-VDS plot of FGPMOS at different values of VGS (-4.5<Vds<-5.5, 0<V_g<4)(b): Id VGS plot of FGPMOS (directly programmable) (V_{ds}= -4.5V, -5<V_{gs}<2) Initial threshold voltage of FGPMOS = +1v.



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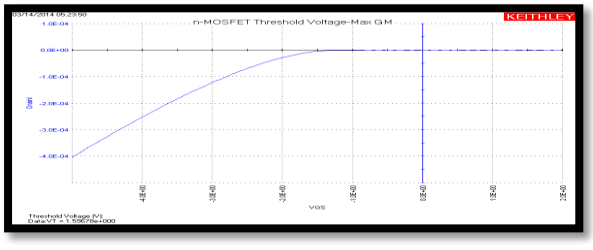


(b)

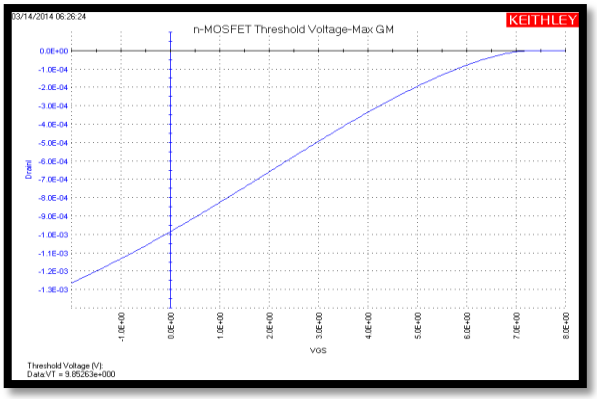
Fig.4. (a): FGPMOS plot demonstrating programming of threshold voltage from 1v to -2v with five successive steps of tunneling from 12v to 13v (b): Id-Vgs plot after 5 successive steps of tunneling (relaxed state).

C. Injection

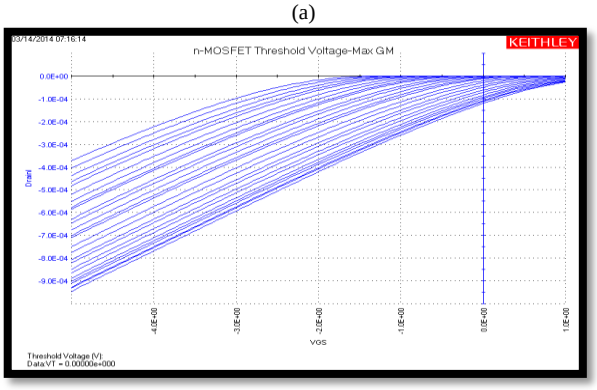
In injection high potential difference between drain and source terminal V_{DS} is sourced from the system through SMUs and change in the value of V_{th} is observed. Injection effect starts when V_{DS} is more than -4.25V. When V_{DS} sourced between -4V to -5V, V_{th} is programmed by about only 0.25V (-1.5V to -1.25V, however between -5V to -6.5V, the value of V_t gets programmed from -1.2V to 7V. After injection when value of drain and source voltage has been sourced at normal conventional values (relaxed state), the value of V_t remain same (=7V), which shows that in absence of any positive potential at V_{Tun} the value of V_{th} remain same at relaxed as stressed state. (as shown in Figure 4(a)).

D. Programming precision

To observed programming precision while tunnelling, V_{Tun} is sourced between 12V to 12.1V with minimum step size of about 4µV (system limitation while sourcing voltage). The change in V_{th} value with least possible change in $V_{Tun}$is about 0.015V ($1/2^6$, 6-bit of resolution) thus we conclude that with tunnelling junction voltage, V_{th} can be programmed with 6-bit of precision. While in injection V_{DS} is sourced between -5V to -5.1V in 26 programming steps (i.e. 4µV step size), the change in value of V_{th} with least possible change in injection voltage is about 0.078V ($1/2^5$), i.e. 5 bit of programming resolution is observed, as demonstrated in I_d-V_{gs} plot in Figure 4(d). The programming range in V_{th} value with injection voltage V_{DS} change is more as compared to the change in V_{th} with similar change in tunnelling voltage V_{Tun} values.



(a)



(b)

Fig.5. (a): FGPMOS char. after 5 successive steps of injection. (b): Plot of FGPMOS demonstrating programming of threshold voltage from -1.5v to 1.5v with 26 successive steps of injection (VDS from -5v to -5.1v).

E. Equilibrium Condition

Both injection and tunnelling mechanism is operated simultaneously and it is being observed that the effect of injection on the charge at the FG (the value of V_{th}) is more as compared to the effect of tunnelling. Equilibrium operating conditions have been obtained where both process effect get nullify. These points are required to substitute operating condition values is design equations required to model this programming processes in FGMOS simulation model (explained in next section), and hence to verify its simulation model.

F. Indirectly programmable FGPMOS

Similarly, the indirectly programmable FGPMOS and FGNMOS designs fabricated in same IC have been characterized and its FG charge is programmed using tunnelling and injection processes. Tunneling is performed using tunnelling junction V_{Tun} and injection is performed using drain source potential difference $V_{DS\_prog\ of}$ programmer PMOS having common FG. The initial V_{th} observed in FGPMOS is equal to -3V and V_{Tun} starts at greater than 11.5V and injection starts beyond -4.5V (V_{DS_prog}>-4.5V). The value of V_{th} can be programmed by about more than 7V to 8V with up to 6 bit of programming precision. Characterizing indirectly programmable FGNMOS and programmer PMOS at same operating biasing condition is very difficult. Thus, before getting initial condition injection is performed and V_{th} value of programmer PMOS is shifted to a positive value. Now characteristic plots of FGNMOS and FGPMOS have been obtained (V_{thn}= 0.05V, V_{thp}=+2.6V). The programming of both V_{th} with tunnelling and with injection due to programmer PMOS have been observed. FGNMOS programming using programmer PMOS is little less efficient as compared to FGPMOS indirect programming using programmer PMOS.

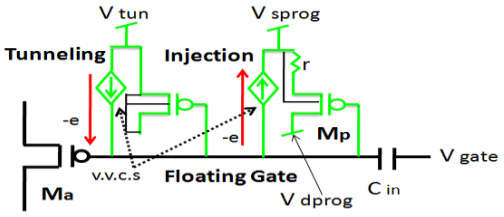


Fig.6.: Simulation model/prototype of indirectly programmable FGPMOS (M_a the FGPMOS, M_p programmer PMOS used for injection, MOS capacitor for Tunnelling, a common FG separated from CG through C_{in} (double ploy structure) and two voltage dependent current sources which depends on current equations (injection I_{inj}& Tunnelling I_{tun} derived from experimental data.).

IV. FGMOS Simulation Model

A. Mathematical modeling using empirical parameters

Simulation model of indirectly programmable FGPMOS shown in Figure 6, consists of input capacitance simulating double poly structure (value 250fF), distinguishing FG with control gate and a tunnelling junction connected with FG through MOS capacitor (drain source substrate of PMOS to tunnelling junction and gate to the FG). The trapped charge on the FGPMOS is altered using two antagonistic quantum mechanical transfer processes: i.e. electrons are removed from the floating gate by Fowler-Nordheim tunneling and added to floating gate by current hot-electron injection (IHEI) from channel to the floating gate across the thin gate oxide. The variation of charge on floating gate can be written as

$$C_F \frac{\partial V_{fg}}{\partial t} = I_{tunnel} - I_{injection} = F_T(V_T, V_{fg}) - F_I(V_d, I_s, V_{fg}) \quad (1)$$

With FGPMOS in saturation its source current is largely expressed as a function of V_{fg}, so that above equation is rewritten with magnitude of I_s absorbed in F_I

$$C_F \frac{\partial V_{fg}}{\partial t} = I_{tunnel} - I_{injection} = F_T(V_T, V_{fg}) - F_I(V_d, V_{fg}).x \quad (2)$$

where binary x is 1 when I_s current flows and 0 otherwise. Variation of I_{tunnel} and $I_{injection}$ is plotted as a function V_{fg} in fig 6. Two salient points characterize the adaptation dynamics of floating gate pFET. V_{fg} above unstable point increases uncontrollably as $I_{tunnel} > I_{injection}$. Below unstable point, V_{fg} always gravitates towards the stable point. Variation in V_T and V_d merely relocates both stable and unstable point. For indirect injection a programmer PMOS at common FG can also be used, shown in Fig 6. Moreover, these tunnelling and injection current are calibrated with voltage controlled current sources whose values depend on externally applied voltages according to the empirical current equations (inspired from [28]). BSIM 3 level 49 MOS parameter file received from foundry is used in FGMOS calibration. From five equilibrium points (when effect of tunnelling is equal to injection effect) from hardware testing, operating conditions (the value of drain, source, tunnelling junction, control gate voltage, estimated FG voltage) is considered and two current equations are equated to form five equations with five constants $(\alpha, \beta, \gamma, \delta, V_f)$ are extracted. The values with 0.5 to 5 percentage of error are considered correct as in the model. The simulation results have also been verified from hardware results. The model is also operated with different simulation environment and technology file.

$$I_{tunnel} = -\delta \exp\left(\frac{-V_f}{V_{(tun-fg)}}\right) \quad (3)$$

$$I_{injection} = I_s \times \alpha \times \exp\left(\frac{-\beta}{V_{(fg-source)}+\gamma} + V_{(source-drain)}\right) \quad (4)$$

Table1: Showing basic simulation results when FGPMOS model is simulated using different MOS model files keeping gate, drain, source and tunnelling junction voltages at V_g=1.5V, V_D= -4.8V, V_S=3V, V_{Tun}=10.4V, W/L= 4.2µm/1.05µm.

MOS model parameter file	BSIM 3 level 49 generic values of 0.35µm	BSIM 3 level 49 received from foundry for 0.35µm	Predictive technology file for 180nm	BSIM 3 for 0.5µm technology
Fixed V_{th}	-0.789 V	-0.921 V	-0.42 V	-0.95 V
Prog. V_{FG}	0.415 V	0.534 V	0.372 V	0.459 V
Time req. to reach equilibrium	2.68 µs	4 µs	3 µs	2.98 µs

B. Model Flexibility

The simulation model of FGMOS has been calibrated with different BSIM 2 level49 parameter files used for 350nm technology, MOS model parameter file used at 180nm technology, model file for 500nm technology. The comparative simulation results have been tabulated in Table 1. The table shows fixed value of V_{th} obtained from respective MOS parameter file, programmed FG voltage (charge at the FG), and the equilibrium time taken by model with different MOS model files. The FG charge takes some time to get stable at a value (about 3 to 4µs) when effect of tunnelling and injection nullify each other (i.e. when $I_{tunelling}$ =$I_{injection}$ in simulation model). The model could not be tested at lower technologies as BSIM 4 parameter file was not operational at simulation tool used. The model is also simulated with different simulation tools (T Spice, Virtuoso, Mentor graphics etc.).

C. Model Features

The model is being verified from hardware results. The model layout/mask consume maximum of 130×90 µm^{2}of chip area. Average power consumed by model is around 0.315mW. FG voltage is completely constant when temperature changes from -50ºC to 150ºC. With on-chip programming of V_{th}, the resistance across FGMOS can also be on-chip tuned, thus the model can be used as on-chip tuneable active resistor. The resistance of the simulation model shows 0.1875Ω/°C sensitivity with changing temperature which would be very less if compared with passive resistors (resistors shows negative temperature coefficient). The model shows noise spectral density of 75nV/Rt (Hz) when 0.25, 1Hz noise is introduced with source voltage (at frequency above 10MHz spectral noise density is equal to 0.025nV/Rt (Hz)). The model shows 13 bit of programming precision in its threshold voltage (or FG charge) programming (0.12mV change in the value of V_{th} when process voltages is sourced).

V. CONCLUSION

The FGMOS transistors have been fabricated using conventional bulk CMOS process. The threshold voltage of fabricated FGMOS can be programmed to any value after fabrication using tunnelling and injection mechanisms. However, with change in V_{th} value beyond 7V to 8 V, it gets very difficult to obtain transistor operating condition. Thus, while programming corner values of tunnelling/injection voltages has been kept such that V_{th} can only be programmed within the transistor operating region value can be programmed with 6 bit of programming resolution/precision. Such precision has been observed with the limitation of sourcing voltage (minimum step size in system 4µV). However, the programming precision can go further, as claimed in previous papers (13-bit and 14-bit programming precision) [7, 8]. The programming is non-volatile and after tunnelling at relaxed state the value of V_{th} is changed by 0.5V as charge at FG gets stable after equilibrium condition is achieved. Programming of charge is controlled and highly stable (temperature change, noise, etc.). The directly programmable FGPMOS of IC_2 is being tested after some time (changed temperature, disturbance due to connecting wires, dust at breadboard and connections), the value of V_{th} remains same as it was when last programmed(=-0.5V).Process variations (offset, mismatches) can also be corrected and thus concept of fault correction and reconfiguring ability can be introduced analog designs. From experimentally observed equilibrium conditions, simulation injection and tunnelling current equations constant values have been derived. The test results have also been compared with pre and post layout simulation results of the model and thus the FGMOS simulation model has been verified. The model is compact, easy to integrate in any analog design, consume less power. FG charge is almost constant with changing temperature and noise.

The model is flexible as being simulated with different MOS parameter files, different technology and at different simulation tools. The model also shows that it can also be operated at higher frequencies (RF range). Instead of optimizing W/L of circuit MOSFETs using iterative steps, the design can be fabricated for basic functionality/ central values of design specification, then using on-chip programming of FGMOSFETs in the circuit, the design specifications value can be accurately tuned to user defined value after fabrication. It reduces design time and accurate prototype of the design can be obtained. The only limitation in such programming is speed. It takes 3 to 4µs of time to reach equilibrium. This precise on-chip programming of circuit transistor's (FGMOSs) characteristics can be highly useful in precision analog signal processing devices and circuits. Additional feedback mechanism in processes can adapt the change of charge at the FG, used to introduce a concept of self-adaption in circuits.

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