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Induction Motor Drive with Trinary DC Source Asymmetrical Inverter

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Abstract*: This paper deals a comparison of MATLAB based simulation of sinusoidal and trapezoidal PWM strategies applied to a trinary DC source nine level inverter fed R - load. The nine-level inverter fed induction motor drive is simulated only for that reference which provides better performance with R- load. Open loop and PI control schemes have also been developed for trinary DC source fed nine level inverter-based Induction motor drive to improve the responses under various sudden load changes at specified reference speed. The corresponding speed, torque and stator voltage are presented. Usual performance indices for transient operation of above drive are also evaluated and presented.

Index Terms: APOD, COPWM, MCPWM, PDPWM

I. INTRODUCTION

Asymmetrical multilevel inverters assure important in the development of industrial drives. The new switching scheme for asymmetrical trinary source inverter. Asymmetrical inverter consists of two H-bridge unit, each unit is fed with different DC sources [1]. The hybrid type asymmetrical inverter is used which simplify the design and control of inverter [2]. The developed high-resolution inverter is used to drive AC machines. The inverter is developed by stacking low level inverter. The stacking of inverter to obtain higher voltage level and also reduce the device voltage and requirement of supply source [3]. The multicarrier pulse width modulation (MCPWM) technique are used for generating gate pulses for NPC- inverters. The developed technique reduces the voltage ripple and implementation is easier than other techniques [4]. Direct torque control technique is used for two phase induction motor drive. Induction motor is powered by four switch inverter and the dynamic performance of the drives are investigated with reference speed [5]. The steady state and transient performance of two-phase induction motor drive are investigated in [6]. The asymmetric multilevel inverter are developed with a main level inverter and auxiliary inverter and both are operated with two different frequencies and supplied by two independent sources [7].

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The voltage controller for drive is designed with PI controller, which improves the system efficiency [8]. Symmetrical binary and trinary multilevel are switched with combined staircase and PWM switching [9].
Torque ripples are reduced by PWM techniques in induction motor drives [10]. Elbouchikhi et al. [11] developed a scheme to detect stator fault in induction motor drive. Permanent magnet synchronous motors (PMSM) are drive with three level inverter. The PMSM drives are controlled by direct torque and flux-controlled method [12]. The multilevel converter with unequal DC supply ratio is used to produce higher stages without modify the original unit [13]. Prabhat et al. [14] reviewed various reduced switch inverter used in different applications and made a comparison of different reduced switched MLI based on their performances. 1:3 voltage ratios are used as a DC source for H –bridge units. Each unit are supplied with separate source of supply and carrier-based switching schemes are used to trigger the switches to achieve desired level of output [15]. The trinary source inverter is triggered with unipolar Pulse width modulation with sine reference. The unipolar sinusoidal pulse width modulation technique provides less %THD [16]. MCPWM techniques are used to solve voltage balancing problem under low frequency conditions [17]. Asymmetric multilevel inverter is triggered with various SPWM technique such as phase disposition, phase opposition disposition and alternate phase apposition disposition [18, 19]. This paper presents simulation studies on Trinary DC source nine level inverter fed resistive load using sine and trapezoidal references for selected carrier arrangements using MATLAB - SIMULIINK. This paper also present open loop and closed loop AC drives with different loading conditions.

II. SINGLE PHASE TRINARY MULTILEVEL INVERTER

The uneven source voltage topology gives greater adaptability to the designer and can create enormous number of levels without expanding the quantity of H-bridge. The trinary nine level inverter chosen has 1:3 DC voltage ratios [1]. The trinary staggered inverter produces nine level voltage with no supplemental multifaceted nature to the current topology with unevenly circulated DC voltages. The trinary nine level inverter comprise of two H-shape modules that are associated in arrangement to accomplish the desired number of voltage levels. Every H-shape module has its very own DC source (VDC and 3VDC) and comprises of four power devices assigned as A_{11}, A_{12}, A_{13} and A_{14} for the primary module and as A_{21}, A_{22}, A_{23} and A_{24} for the subsequent module (Fig. 1).

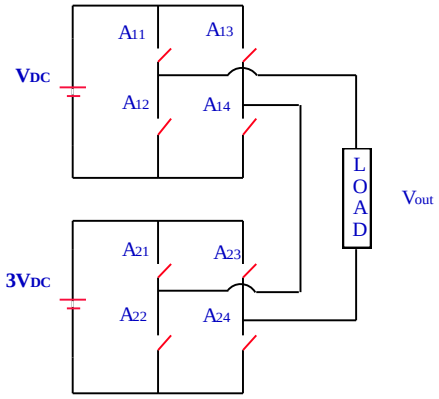


Fig. 1 Trinary nine level inverter.

The upper module produces a voltage with three levels, and after that, the lower module includes or subtracts one stage from the essential wave to integrate ventured waves. Here, the voltage levels become the aggregate of every terminal voltage of the H-shape module.

Table 1 archives the attained voltage with the relating firing states. Figs. 2 (a - i) show respectively the switching strategies to synthesize various levels.

Table 1 Firing states.

A_{11}	A_{12}	A_{13}	A_{14}	A_{21}	A_{22}	A_{23}	A_{24}	*Level*
on	off	off	on	on	off	off	on	+4L
off	on	off	on	on	off	off	on	+3L
off	on	on	off	on	off	off	on	+2L
on	off	off	on	off	on	off	on	+1L
off	on	off	on	off	on	off	on	0
off	on	on	off	off	on	off	on	-1L
on	off	off	on	off	on	on	off	-2L
off	on	off	on	off	on	on	off	-3L
off	on	on	off	off	on	on	off	-4L

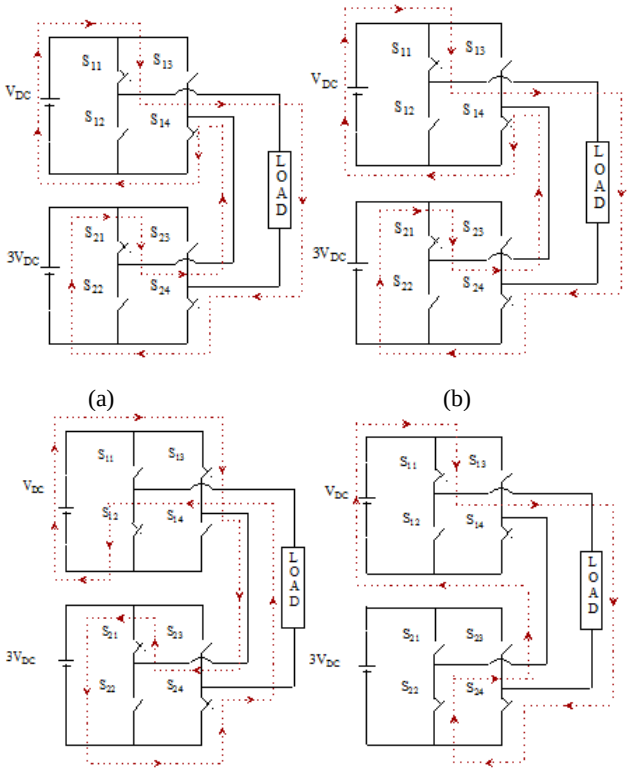


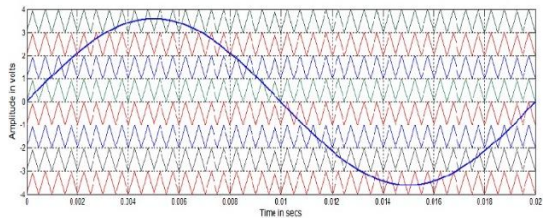
Fig. 2. Switching strategy to generate output voltage level and load current path.

(a) 4L. (b) 3L. (c) 2L. (d) 1L. (e) 0. (f) −L. (g) −2L. (h) −3L. (i) −4L.

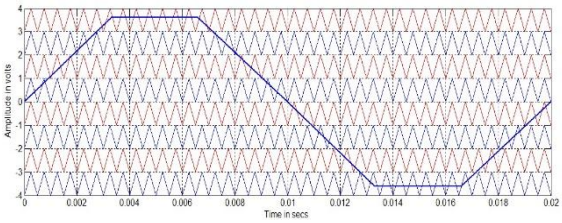
III. MODULATION STRATEGIES FOR TRINARY SOURCE NINE LEVEL INVERTER

In this work Multicarrier based triggering methodologies for this trinary source fed induction motor drive of nine level inverter is developed using MATLAB for PDPWM, APODPWM, COPWM and VFPWM strategies with bipolar triangular carrier arrangements using two different reference such as sine and trapezoidal.

MCPWM strategies uses one reference (sinusoidal/ Trapezoidal) and eight carrier signals (triangular) with same magnitude and same frequency [20]. The carrier waves are structured above and underneath the modulated wave. By comparing sine/ Trapezoidal signal with triangular signal, it generate command signals (A1, A2….A8). The switching signals are generated by logical combination of command signal. Carrier arrangements are displayed only for a Phase disposition approach with sine and trapezoidal wave. Fig. 3 shows the reference and carrier wave pattern for MCPWM methodology.



(a)



(b)

Fig. 3 MCPWM methodology
(a) Sine wave with triangular carrier.
(b) Trapezoidal reference with triangular carrier

IV. SIMULATION RESULTS OF TRINARY NINE LEVEL INVERTER WITH R - LOAD

Trinary multilevel inverters and control methodologies are developed in SIMULINK environment. Fig. 4 and 5 separately demonstrate the nine-level voltage produced by APODPWM strategy, which provides relatively minimum THD with sinusoidal reference and its harmonic spectrum for m_a = 0.9. Fig. 6 and 7 display the nine-level voltage produced by APODPWM methodology with trapezoidal reference and its FFT plot for modulation index 0.9. The accompanying parameter are utilized: DC Supply of 75V and 225V, 100 ohms Resistive load, carrier frequency of 2000 Hz and modulated frequency of 50Hz.

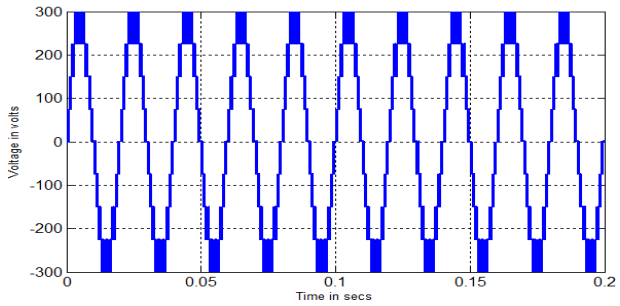


Fig. 4 Voltage created by APODPWM technique with sinusoidal reference

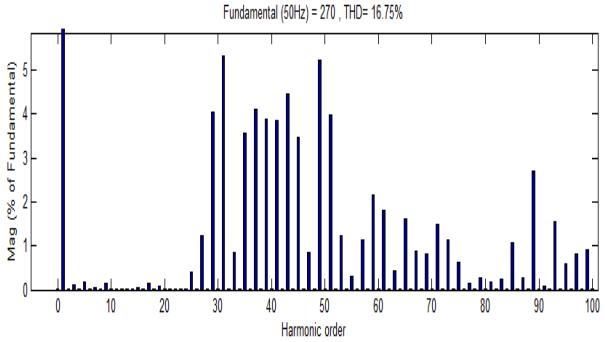


Fig.5 Harmonic spectrum

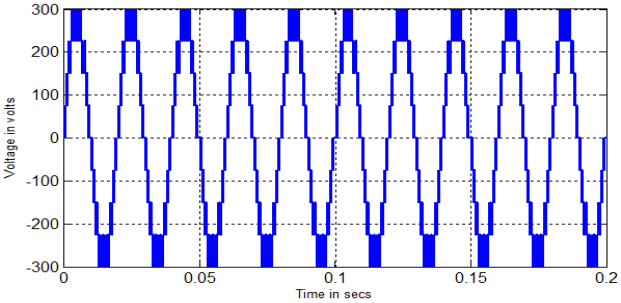


Fig.6 Voltage created by APODPWM technique with Trapezoidal reference

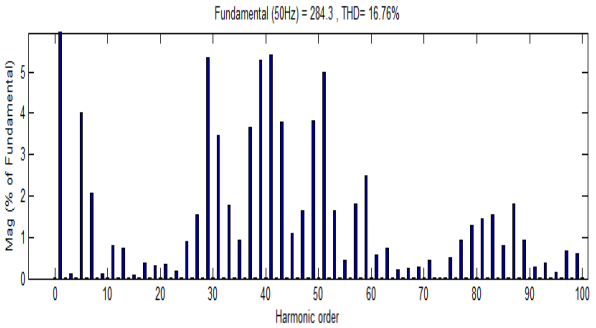


Fig.7 Harmonic spectrum

Table 2 % Total Harmonic Distortion

m_a	Sinusoidal Ref.				Trapezoidal Ref			
	PDPWM	APODPWM	CO PWM	VF PWM	PD PM M	APOD PWM	CO PWM	VF PWM
1	13.44	13.33	18.18	15.16	11.75	12.11	16.68	13.33
0.95	15.66	15.64	19.97	16.81	15.03	15.24	19.37	16.74
0.9	16.76	16.75	22.03	17.35	17.01	16.76	21.12	18.34
0.85	16.94	16.93	23.76	17.20	17.72	17.75	22.85	17.59
0.8	16.97	16.22	26.16	17.28	17.17	17.52	24.15	16.21

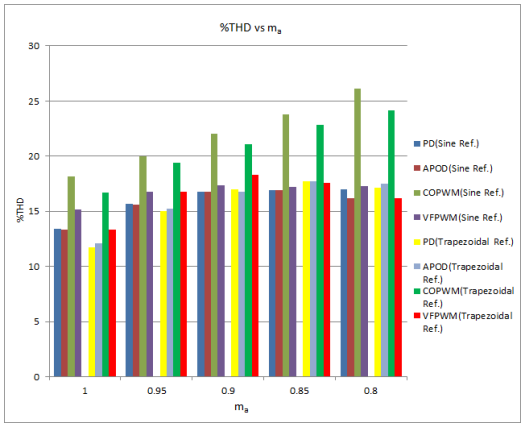


Fig. 8 %THD of output voltage vs m_a

Table 3 Output voltage response

ma	Sinusoidal Ref.				Trapezoidal Ref			
	PDPWM	APODPWM	CO PWM	VF PWM	PD PWM	APOD PWM	CO PWM	VF PWM
1	212.6	211.8	217.4	212.4	223.2	223.2	225.7	221
0.95	201.6	201.7	209.2	200.3	212.6	212	217	211.6
0.9	190.6	190.9	199.9	189.5	201.4	201	208.2	202.1
0.85	179.6	180.3	190.2	179	189	190.2	199	191.9
0.8	169.6	169.3	178.7	168.3	178.2	178.7	189.6	179.8

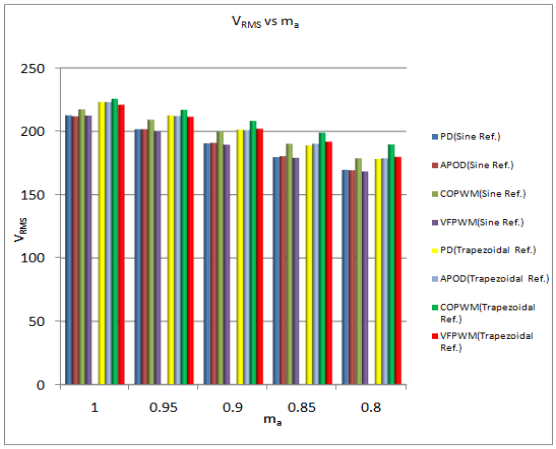


Fig. 9 RMS output voltage (fundamental) vs ma

Table 4 %DF for different modulation indices

ma	Sinusoidal Ref.				Trapezoidal Ref			
	PDPWM	APOD PWM	CO PWM	VF PWM	PD PMM	APOD PWM	CO PWM	VF PWM
1	0.0261	0.0215	0. 1717	0.0006	0.1550	0.1604	0.2977	0.0019
0.95	0.0585	0.0143	0. 2452	0.0007	0.1706	0.1606	0.3264	0.0023
0.9	0.0156	0.0168	0. 3758	0.0016	0.1774	0.1667	0.3963	0.0026
0.85	0.0568	0.0163	0. 528	0.0021	0.1806	0.1693	0.54	0.0029
0.8	0.0379	0.0103	0. 6314	0.0018	0.1832	0.1707	0.6737	0.0028

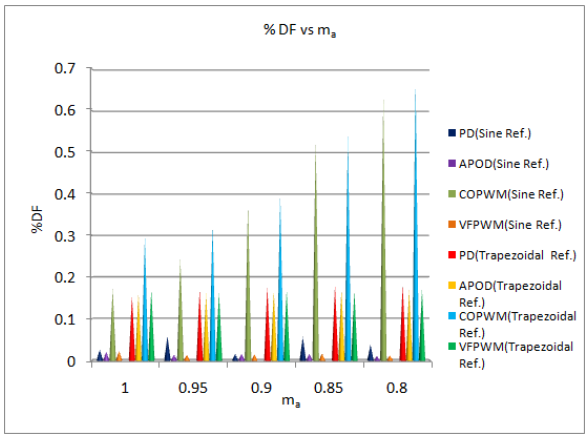


Fig. 10 % Distortion factor

It is seen that on account of MCPWM methodologies (i) the harmonic content of the output voltage is relatively least for APODPWM scheme with sinusoidal reference (Table 2 and Fig. 8) (ii) the carrier overlapping scheme offers the maximum DC bus utilization and all other strategies have comparatively same (Table 3 and Fig.9) and (iii) VFPWM strategy with sinusoidal reference has lower % DF (Table 4 and Fig.10). The stress on the device is indicated by CF and it is calculated for all the above strategies for various modulation indices. It is found that the value is nearly same for all the strategies and is equal to 1.414.

V.PI BASED SPEED LOOP CONTROLLER FOR INDUCTION MACHINE

AC induction motor has many advantages over DC motor. Hence the induction motor is preferred for drive applications. PI controller has been utilized for a wide scope of control applications with near optimal performance and due to simplicity. The nine level output of the inverter is fed to the motor load. Fig. 11shows the Block outline for MLI with PI mechanism. Speed of the motor (w_r) is contrasted with the set speed (w_{ref}) to create the error signal (e). The contribution to the PI controller is e. The output of the PI controller i.e the remunerating signal C_S is summing with W_{ref} to deliver the supervisory signal m_s which when connected as reference to MCPWM to produce the perfect activating signals.

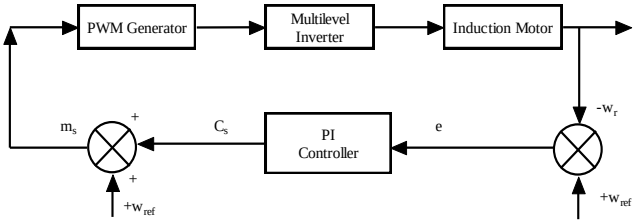


Fig. 11 Block diagram for MLI with PI control

VI. SIMULATION RESULTS OF TRINARY NINE LEVEL INVERTER FED INDUCTION MOTOR DRIVE

The presentation of the nine level trinary inverter for induction motor drive exhibited above has been confirmed by simulation.

0.25 HP, 110V, single phase IM has been taken and its rated parameters are Rs: 1.3522 Ohms, Rr: 2.758 Ohms, Lis: 0.0049537 H, Llr: 0.0037487 H, Lm: 0.11862 H, J: 0.0146 kgm2 and Pole pairs:2. The simulations were performed with MATLAB-Simulink. Switching signals are developed using the best performing reference in R - load. APODPWM strategy using sinusoidal reference is used to create the firing signals for the inverter. The simulations are performed both in open loop and closed loop modes of operation. The various performance characteristics such as torque, speed and voltage are observed. Fig. 12 shows the open loop response of start-up transients of speed and torque of chosen IM drive. Figs. 13 and 14 demonstrate the open loop reaction of inverter voltage and its harmonic spectrum.

Figs. 15 - 20 show the transients in speed, torque and inverter output voltage and its harmonic spectrum with rapid load variations from no load to graded load (0 N-m to 1.5 N-m) at t = 2 sec and vice versa in the open loop mode.

Fig. 21 shows the closed loop response (with PI controller) of speed and torque of chosen IM drive. Fig. 22 and Fig. 23 show the closed loop response of inverter output voltage and its FFT plot. Figs. 24 - 29 show the transients in speed, torque and inverter output voltage and its FFT plot with rapid load variations from no load to graded load (0 N-m to 1.5 N-m) at t = 2 sec and vice versa in the closed loop mode.

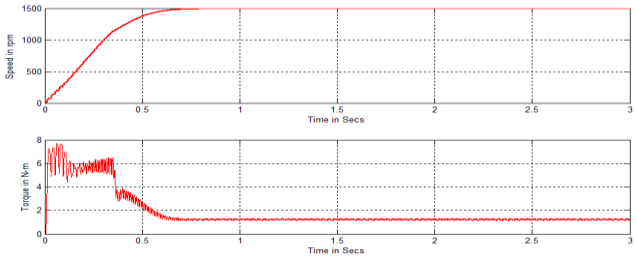


Fig.12 Speed and Torque response without controller

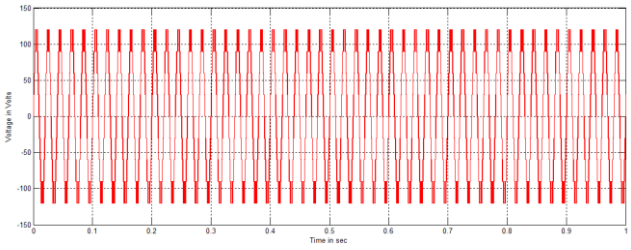


Fig.13 Voltage response of trinary inverter

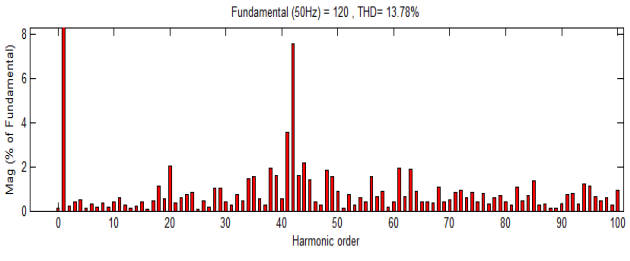


Fig.14 Voltage harmonic spectrum

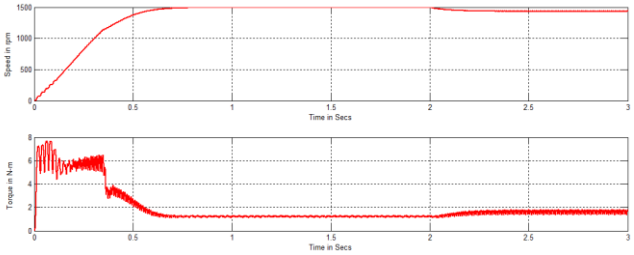


Fig. 15 Speed and Torque response without controller with variable load torque (0 N-m to 1.5 N-m).

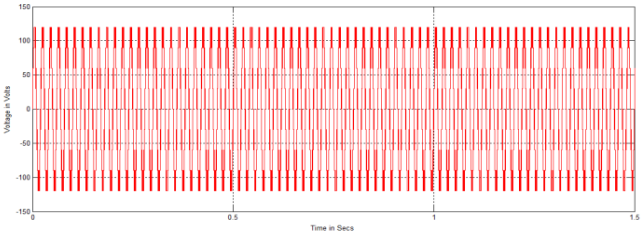


Fig.16 Voltage response of trinary inverter

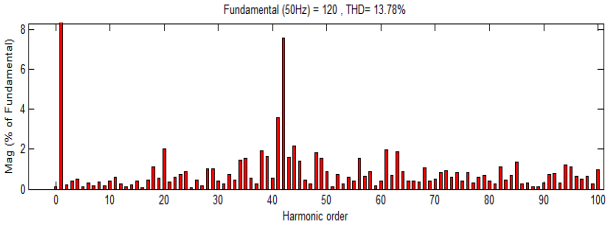


Fig.17 Voltage harmonic spectrum

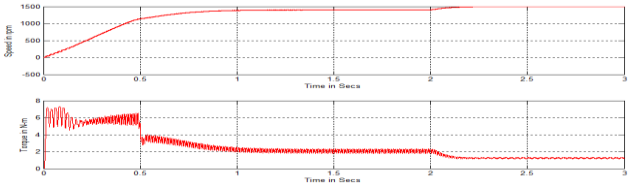


Fig. 18 Speed and Torque response without controller with variable load torque (1.5 N-m to 0 N-m)

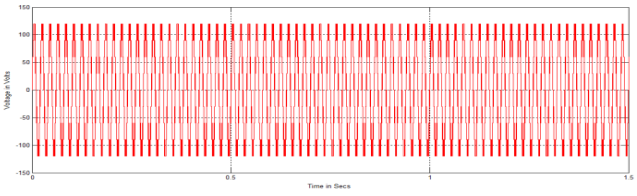


Fig.19 Voltage Response of trinary inverter

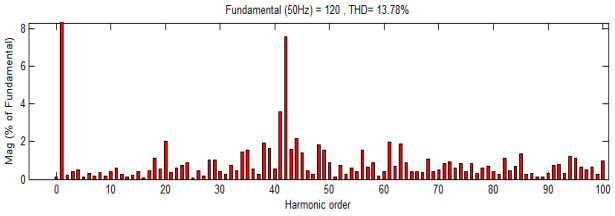


Fig.20 Voltage harmonic spectrum

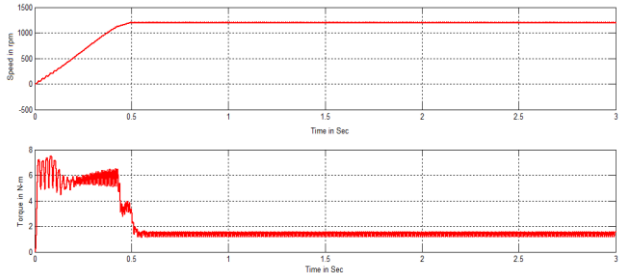


Fig. 21 Speed (rated speed=1250 rpm) and Torque response of closed loop System

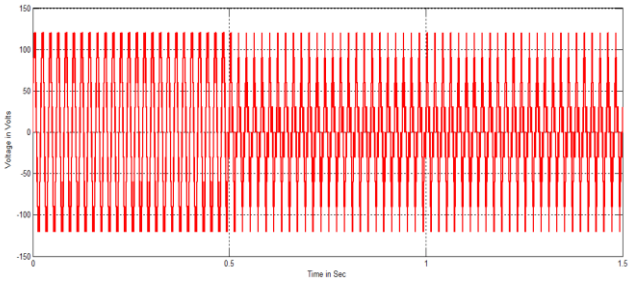


Fig.22 Voltage Response of trinary inverter

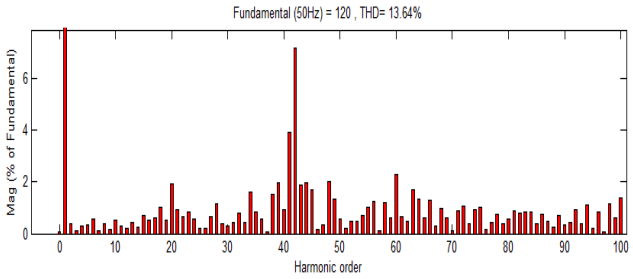


Fig.23 Voltage harmonic spectrum

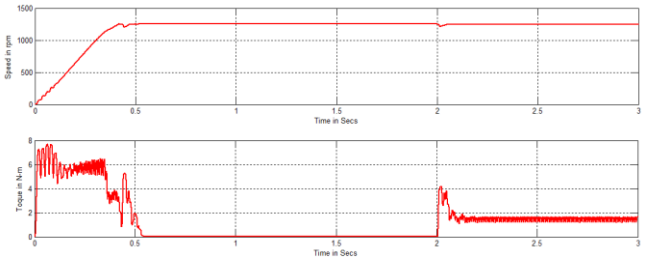


Fig. 24 Speed (rated speed=1250 rpm) and Torqu response of closed loop system with variable load torque (0 N-m to 1.5 N-m).

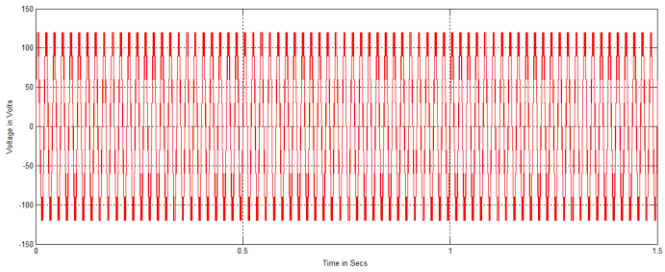


Fig.25 Voltage Response of trinary inverter

Fig.26 Voltage harmonic spectrum

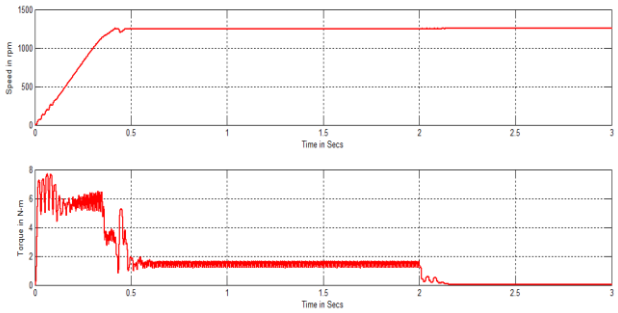


Fig.27 Speed (rated speed=1250 rpm) and Torque response of closed loop system with variable load torque (1.5 N-m to 0 N-m).

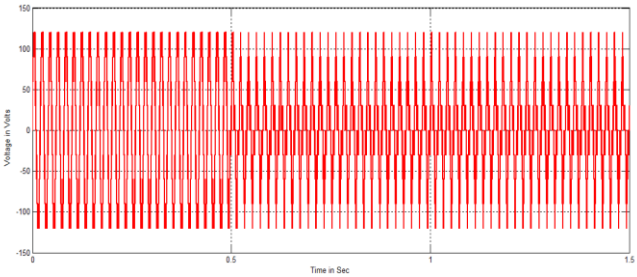


Fig.28 Voltage Response of trinary inverter

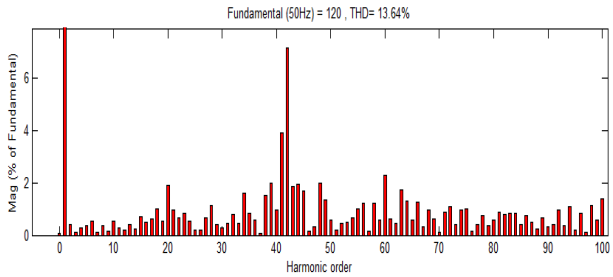
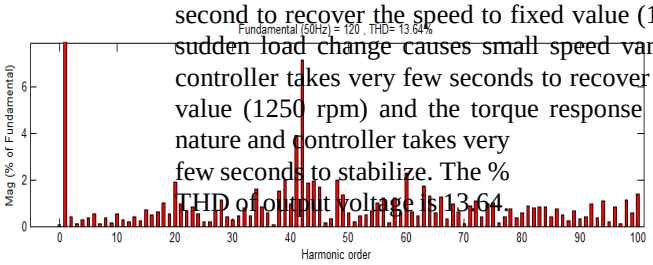


Fig.29 Voltage harmonic spectrum

From the simulation result of open loop mode, it is inferred that the machine speed is zero and torque is high and after 0.8 second the motor reaches steady state speed (Fig. 12). Hence electrical torque is equal to mechanical torque. The % THD of output voltage is 13.78 (Fig. 14). Further it is observed from Figs. (15 – 20) the machine accelerated under no load to rated load (0 N-m to 1.5 N-m) and vice versa. Under no load condition, machine is accelerated to rated1500 rpm. Then 1.5 N-m load is added to the machine the speed drops to 1460 rpm and vice-versa. The output voltage THD is 13.78% in both loading conditions. From the simulation results of closed loop mode, it is inferred that the motor speed increases linearly up to the set speed of 1250 rpm in 0.45 second as shown in Fig. 20. After 0.5 second, the speed stabilizes at set speed. The % THD of output voltage is 13.64 (Fig. 23). Further it is observed from Figs. (24 - 29) the controller proceeds 0.5 second to recover the speed to fixed value (1250 rpm) and a sudden load change causes small speed variations then the controller takes very few seconds to recover the speed to set value (1250 rpm) and the torque response is oscillatory in nature and controller takes very few seconds to stabilize. The % THD of output voltage is 13.64.



VII. CONCLUSION

Chosen trinary source fed nine level AMLI based R-load and induction motor drive are developed and presented. A PI based control methodology is also developed to regulate the speed of the above drive. The closed loop responses of the drive system have been obtained under different loading conditions. The results are presented and analyzed and are satisfactory.

REFERENCES

1. V. Arun, B. Shanthi, and S. P. Natarajan, "'Investigation of Digital Control Strategy for Trinary DC Source Cascaded Multilevel Inverter,'" *Int. J. Emerg. Trends Eng. Dev.*, vol. 1, no. 3, pp. 382–390, 2013.
2. S. Mariethoz, "Design and control of high-performance modular hybrid asymmetrical cascade multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 4018–4027, 2014.
3. V. R. Nair, K. Gopakumar, and L. G. Franquelo, "A very high resolution stacked multilevel inverter topology for adjustable speed drives," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2049–2056, 2018.
4. L. Tan, B. Wu, M. Narimani, D. Xu, and G. Joos, "Multicarrier-Based PWM Strategies with Complete Voltage Balance Control for NNPC Inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 2863–2872, 2018.
5. A. Ouarda, B. El Badsi, and A. Masmoudi, "Bus-Clamping-Based Direct Torque Control Strategy Dedicated to B6-Inverter Fed Symmetrical Two-Phase im Drive," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5344–5352, 2018.
6. A. Ouarda, B. El Badsi, and A. Masmoudi, "Direct RFOC Strategies Aimed to Symmetrical Two-Phase im Drives: Comparison between B4-and B6-Inverters in the Stator," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9772–9782, 2018.
7. S. Foti *et al.*, "An Optimal Current Control Strategy for Asymmetrical Hybrid Multilevel Inverters," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4425–4436, 2018.
8. Wenxiang Zhao , Peng Zhao, Dezhi Xu, Zhonghua Chen and Jihong Zhu, "Hybrid Modulation Fault-Tolerant Control of Open-End Windings Linear Vernier Permanent-Magnet Motor with Floating Capacitor Inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2563–2572, 2019.
9. J. Perez Ramirez, J. A. Beristain Jimenez, J. H. Hernandez Lopez, and R. F. Urquijo Ramos, "Hybrid Modulation Strategy for Asymmetrical Cascade H-Bridge Multilevel Inverters," *IEEE Lat. Am. Trans.*, vol. 16, no. 6, pp. 1623–1630, 2018.
10. N. K. Bajjuri and A. K. Jain, "Torque Ripple Reduction in Double-Inverter Fed Wound Rotor Induction Machine Drives Using PWM Techniques," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4250–4261, 2019.
11. E. Elbouchikhi, Y. Amirat, G. Feld, and M. Benbouzid, "Generalized likelihood ratio test based approach for stator-fault detection in a PWM inverter-fed induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 6343–6353, 2019.
12. G. H. B. Foo, T. Ngo, X. Zhang, and M. F. Rahman, "SVM Direct Torque and Flux Control of Three-Level Simplified Neutral Point Clamped Inverter Fed Interior PM Synchronous Motor Drives," *IEEE/ASME Trans. Mechatronics*, vol. 24, no. 3, pp. 1376–1385, 2019.
13. G. Irusapparajan, D. Periyaazhagar, N. Prabaharan, and A. Rini ann Jerin, "Experimental verification of trinary DC source cascaded H-bridge multilevel inverter using unipolar pulse width modulation", Automatika vol. 60, no. 1 pp.: 19-27, 2019.
14. P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano, and G. Panda, "Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application: Topologies, Comprehensive Analysis and Comparative Evaluation," *IEEE Access*, vol. 7, pp. 54888–54909, 2019.
15. A. Sinha, M. K. Das, and K. C. Jana, "Control of asymmetrical cascaded multilevel inverter for a grid-connected photovoltaic system," *IET Renew. Power Gener.*, vol. 13, no. 9, pp. 1456–1465, 2019.
16. V. Arun, B. Shanthi, and A. Bharathi, "Performance Evaluation of Various Unipolar SPWM Strategies of Trinary DC Source Multilevel Inverter," *Int. J. Eng. Innov. Technol.*, vol. 2, no. 6, pp. 458–462, 2012.
17. L. Tan, B. Wu, M. Narimani, D. Xu, and G. Joos, "Multicarrier-Based PWM Strategies with Complete Voltage Balance Control for NNPC Inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 2863–2872, 2018.
18. R. A. Vargas, A. Figueroa, S. E. Deleon, J. Aguayo, L. Hernandez, and M. A. Rodriguez, "Analysis of Minimum Modulation for the 9-Level Multilevel Inverter in Asymmetric Structure," *IEEE Lat. Am. Trans.*, vol. 13, no. 9, pp. 2851–2858, 2015.
19. N. Prabaharan, K. Palanisamy and A. Rini ann jerin, "Asymmetric Multilevel inverter structure with hybrid PWM strategy" *International Journal of Applied Engineering Research*, vol. 10, no. 55, pp.: 2672-2676, 2015.
20. N. Prabaharan and K. Palanisamy, "Modeling and analysis of a quasi-linear multilevel inverter for photovoltaic application", *Energy Procedia*, vol. 103 pp.: 256-261, 2016.

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