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Stability analysis of Sub-threshold 6T SRAM cell at 45 nm for IoT application

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Abstract: ***In ultra-Low power application the supply volt- age in the circuit is as minimum as possible to correct perform the operation. Reducing the supply voltage below the threshold Voltage of transistor is known as sub threshold voltage that affects the delay as well as stability parameter of the Circuit. In this paper body biased technique is applied at standard 6T SRAM which improve the static Current Noise Margin(SINM) and Write trip Current by the factor of 4.15 times and 4.7 times respectively from the Conventional (conv) 6T SRAM. SINM defined the read stability whereas WTI are write ability Parameters of the circuit. In the Sub threshold region delay parameter of the circuit increased, but in this paper delay and power of the proposed circuit are going to be degrades 2.34 times and 4.39 times from the conv. 6T SRAM at different Process Corner i.e. the Performance of the device get increased. In this paper conventional (Conv.)6T and Proposed(PP) 6T both have same W/L ratio at supply voltage of 400mv.***

Index Terms: ***Sub-threshold region, Read stability, Write ability, Process Corners, Body biasing***

I. INTRODUCTION

Static Random Access memory (SRAM) played a very important role for in the field of Internet of Things (IoT). IoT is a system that connects the digital world at very low power. There are many applications where IoT works such as wearable electronics, robotics, wireless sensor nodes, biomedical equipment etc. In this system performance of the system is secondary need whereas Power is the main concern for that system. Reducing the supply voltage is very easy for less power dissipation but the device not work properly. Another way for Ultra Low Voltage(ULV) system, Sub-threshold logic SRAM cell is one of the conceivable choices to minimize the standby power in the circuits, but the main limitation associated with sub-threshold region is poor read stability or feeble write ability [2].In the sub threshold SRAM the operation of transistor is totally different from super threshold region. Maintaining the SRAM parameter likewise stability, delay is quite difficult in the sub-threshold region. To improve the stability Schmitt trigger based SRAM is used which operates properly at ULV [12]. In under threshold region sub threshold leakage current are used as operating current of the transistor.In this region the active power dissipation degrades quadratically [10].It can be observed that as the channel length is going to be de- grades the Leakage power get increases at nanometer technology [9].

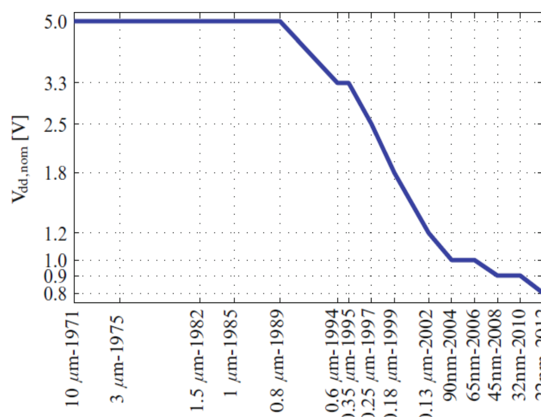

Fig 1: Technology and Introducing year [7]

SRAM is the storing device in which latching circuitry is used to store the information. A conventional SRAM used six transistor in which four transistor form two inverter which is connected in series. Mainly these back to back inverter have stored the bit. This circuitry have store the bit in two states which are complementary of each other as shown in fig.2.A part from latch circuitry two access transistors are used to control the signal amid reading and write tasks. SRAM is worked as temporary storing devices and used as cache memory [11]. Notwithstanding such SRAM, other design of SRAM that is 7T, 8T, 9T and 10T SRAM are used to improve the performance and stability but have penalty of area of the gadgets. Moreover, when SRAMs work under below the operating voltage, alpha-particles or energetic cosmic beams can possibly prompt soft errors in the circuit [6].To reduce soft error rate in the circuit bit-interleaving structure with error correction code is implemented simultaneously [8], [3]. This paper is organized as follows: The conventional 6T and Proposed 6T SRAM is discussed in section II. Section III Covers the simulation result which include "Static Voltage noise Margin(SVNM),Static Current noise Margin(SINM),Write trip Voltage (WTV) Write trip Current(WTI)",Read delay, Read power, Write delay, Write Power at different Corner analysis. Finally, Conclusion are discussed in section IV

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II. SRAM CELL

The conventional 6T SRAM is the basic structured of memory system. It consist of two inverter which is connected in the form a latch structure to store the information as shown in figure:2

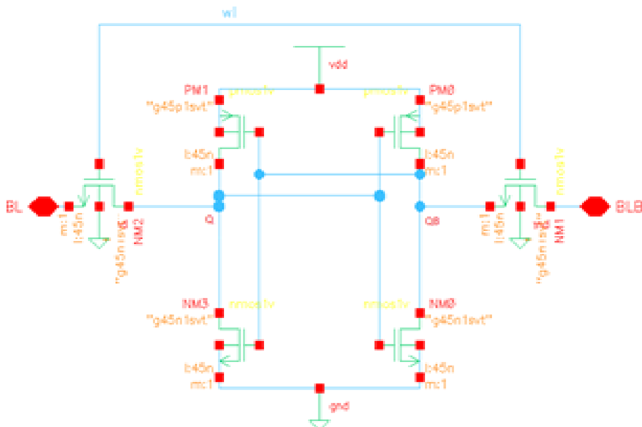

Fig. 2 Conventional 6T SRAM

Two access transistor is used which is provide the read and write operation in memory cell. Widths of the transistor are main design consideration of SRAM cell. It defines by help of α, and β term. α is the ratio between width of Pull up transistor and Width of access transistor whereas β is the ratio between width of Pull down transistor and Width of access transistor To avoid the read upset the value of α lies in between 1.2 to 3 and the values of β is less than 1.8 is required [4]. During read operation both BL and BLB as well as WL are connected to Vdd .The access transistor is provide the path to one of the bit-line for discharging the node voltage. During write operation WL is connected to logic 1 and One of the bit-line is connected to ground and other is connected to Vdd which helps to write within the cell.

A. *Proposed (PP) 6T SRAM*

In this circuit body biasing technique is used which effects the threshold voltage of the transistor. This circuit is different from the conventional 6T SRAM, in this manner that the body voltage of left side inverter is connected to the through- put of the right side inverter (MP2 and MN5) which work as inverter as well as body biasing circuit. Because of the charging and discharging of the storage node of the cell is fastly. Which improve the speed as well as stability of the circuit.In this design read, write and hold operation is same as conventional 6T SRAM. In the read operation wordline (WL) is connected to V_{DD} and both the bitline (BL and BLB) are pre- charged. Assume that the Q has store the logic low .The data at storage Q turns on the PMOS (PM2) whereas turn off the NMOS (NM5) it means the storage node QB is connected to V_{dd} which doesn't discharge the BLB because the potential difference is not developed on the other hand the storage node QB is connected to the left inverter which tern ON the NMOS (NM6) and providing a discharging path through

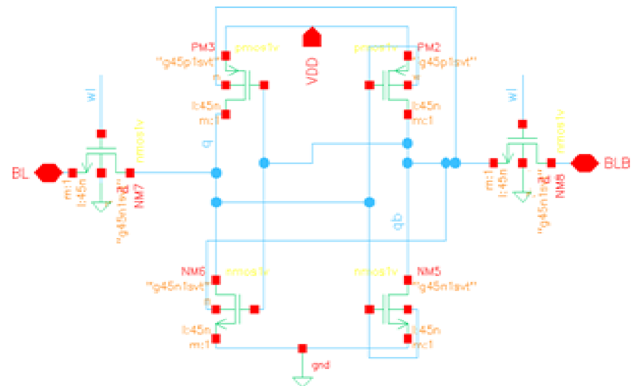

Fig. 3 PP 6T SRAM

NM7 to NM6.If the voltage difference between both the bit-line(BL and BLB) is more the 50mv [8].The sense amplifier sense logic 0 which have lowest voltage and other is logic 1.

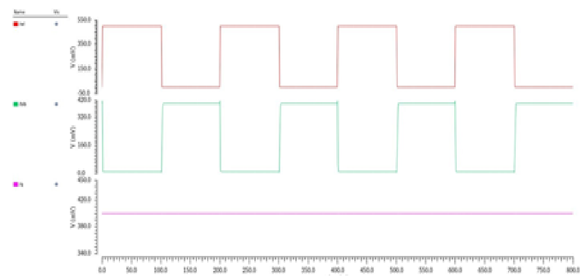

Fig. 4 Read wave form of PP 6T SRAM

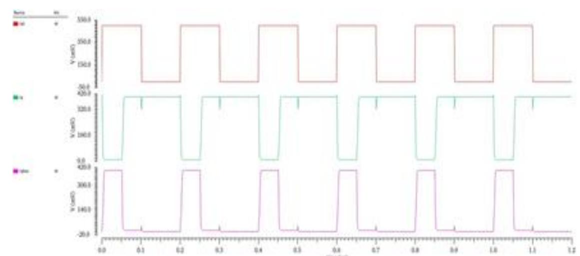

Fig. 5 Write wave form of PP 6T SRAM

Write operation is performed when the one the bitline is clamped to ground and other is clamped to Vdd and WL is connected to Vdd .Assume that BL is clamped to Vdd and BLB is connected to ground. When the WL is turn on the voltage of BL comes at the storage node Q which effects the right hand inverter i.e. NMOS (NM5) is on by the help of this at the storage node QB logic 0 is written. This logic 0 turns the PMOS (PM3) and logic 1 is written at Q. In the hold operation the WL is turned off which disconnect the bit-line from the storage node and the memory is in idle state

III. SIMULATION RESULTS

In this section proposed SRAM is compare with the conventional SRAM with different parameter likewise Write ability (WTI and WTV) Read stability (SVNM and SINM),read delay, write delay, ,read power, write power at different corner analysis at supply voltage of 400mv.

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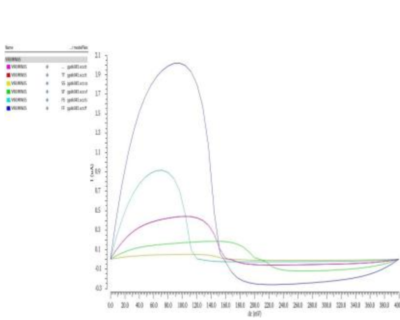
Figure 6: Stability analysis of Convention SRAM

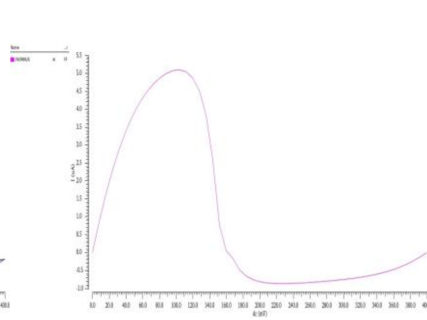
Figure 7: Stability analysis at FF corners PP. 6T SRAM

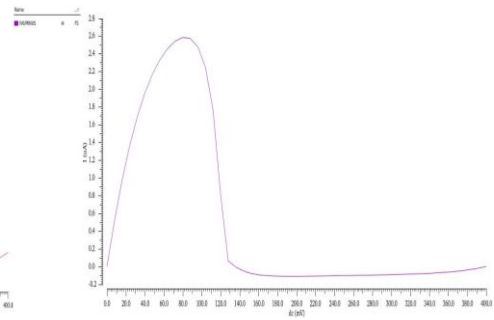
Figure 8: Stability analysis at FS corners PP. 6T SRAM

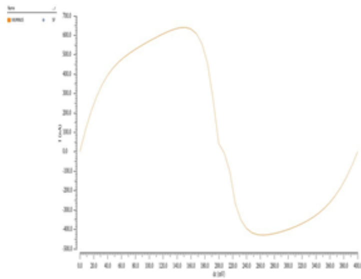
Figure 9: Stability analysis at SF corners P P.6T SRAM

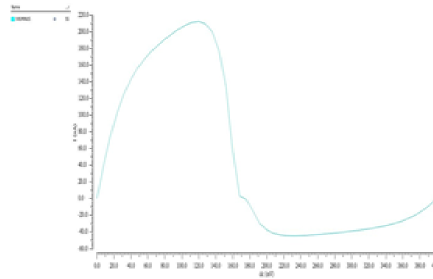
Figure 10: Stability analysis at SS corners of PP. 6T SRAM

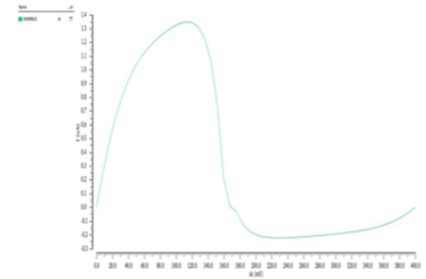
Figure 11: Stability analysis Of TT corner of PP. 6T SRAM

A. *Stability Analysis*

The stability of SRAM cell is usually calculated by the butterfly curve which provides the static noise margin (SNM) of the circuit. SNM is defined as the maximum noise voltage that can be handled by the circuit, but It doesn't provide the statistical information as well as Static Current Noise Margin (SINM) of SRAM cell. An alternative method to find the stability of the cell is N-curve method which provide the Current as well as Voltage of the noise margin of the circuit [5], [1].Stability of the circuit is extracted through the N-curve when both the bit-line clamped to V_{dd} and access transistor are ON.A voltage swipe from 0 to V_{dd} is applied at the storage node the cell to find the stability of the cell. N-curve graphs cross the zero line at three points. The potential difference between these cutting points provides the volt- age noise margin and peak current show the current noise margin of the circuit. Larger the peak current better will be stability of the circuit. As the supply voltage is scaled down the stability of the circuit degrades.

Table 1: Read Stability of conv.6T SRAM at different Process Corners

Process Corners	Conv. 6T SRAM	
	SVNM(mv)	SINM(μA)
TT	163	0.442
FF	156	2.020
SS	166	0.051
FS	120	0.916
SF	206	0.186

In this paper stability analysis has done different corner analysis i.e. "FF (Fast NMOS Fast PMOS), SS (Slow NMOS Slow PMOS), FS (Fast NMOS Slow PMOS), SF (Slow NMOS Fast PMOS) and TT is the nominal Corner". Read stability and Write ability of Proposed(PP) SRAM at all Process Corner is 3.05 to 4.15 times and 3.30 to 4.77 times respectively better than Conv. 6T SRAM respectively.

Table 2: Read Stability of PP 6T SRAM at different Process Corners

Process Corners	PP. 6T SRAM	
	SVNM(mv)	SINM(μA)
TT	168	1.350
FF	160	5.100
SS	171	0.212
FS	133	2.581
SF	206	0.641

Table 3: Write ability of conv.6T SRAM at different Process Corners

Process Corners	Conv. 6T SRAM	
	WTV (mv)	WTI (nA)
TT	237	58.65

FF	244	262.36
SS	234	9.310
FS	280	26.58
SF	194	121.72

Table 4: Write ability of PP. 6T SRAM at different Process Corners

Process Corners	PP. 6T SRAM	
	WTV (mv)	WTI (nA)
TT	232	221.5
FF	240	866.6
SS	229	044.5
FS	267	108.8
SF	194	429.0

B. Delay and Power analysis of SRAM

In the weak inversion region supply voltage of the circuit is scaled down below the operating Voltage of the transistor due that delay of the circuit increases and power consumption of the devices gets reduced. From table 5 & 6 it has been seems that delay and Power of the Proposed SRAM get reduced 1.03 to 2.34 times and 1.26 to 4.39 as comparison to conv. 6T respectively. In the sub threshold delay parameter is

Table 5: Read delay at different Process Corner

Process Corners	Conv. 6T SRAM Read delay	PP. 6T SRAM Read delay
TT	554.1ps	516.3ps
FF	380.7ps	366.6ps
SS	1.273ns	850.9ps
FS	420.0ps	405.0ps
SF	1.572ns	669.9ps

Table 6: Read power at different Process Corner

Process Corners	Conv. 6T SRAM Read Power	PP. 6T SRAM Read Power
TT	561.0pw	388.0pw
FF	2.420nw	1.775nw
SS	248.7pw	196.6pw
FS	216.0pw	113.5pw
SF	13.46nw	3.063nw

Table 7: Write delay at different Process Corners

Process Corners	Conv. 6T SRAM		PP. 6T SRAM	
	Write 0	Write 1	Write 0	Write 1
TT	738.6ps	3.514ns	738.6ps	3.514ns
FF	100.2ns	602.8ps	100.2ns	602.8ps
SS	2.29 ns	20.40ns	2.290ns	20.40ns
FS	557.6ps	6.760ns	557.6ps	6.760ns
SF	1.492ns	3.220ns	1.492ns	3.22 ns

Delay and Power of the Proposed SRAM get reduced 1.03 to 2.34 times and 1.26 to 4.39 times as comparison to conv. 6T respectively. In the sub threshold delay parameter is

Table 8: Write Power at different Process Corner

Process Corners	Conv. 6T SRAM Write Power	PP. 6T SRAM Write Power
TT	4.031nw	4.031nw
FF	4.930nw	4.930nw
SS	3.020nw	3.020nw
FS	4.080nw	4.080nw
SF	5.610nw	5.610nw

major challenges of any circuit. In the SRAM cell write delay is defined as how much time taken by the cell to change the state of storage node. In table 7 & 8 it seems that delay and power consumption is same as conv.6T SRAM

IV. CONCLUSION

This paper presents a robust, low power, high noise handling SRAM cell. The proposed SRAM cell is analyzed at different Process Corners on Various parameters likewise SVNM, SINM, WTV, WTI, Delay and Power. Proposed 6T SRAM cell has better static current noise margin i.e. read stability than the Conv. 6T circuit. Performance of the proposed circuit is better with low power dissipation in comparison from Conv.6T SRAM. Therefore the Proposed circuit is viable choice for IoT based applications.

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REFERENCES

1. D Anitha, K Manjunatha Chari, and P Satish Kumar. N-curve analy- sis of low power sram cell. In 2018 Second International Conference on Inventive Communication and Computational Technologies (ICI-CCT), pages 1645–1650. IEEE, 2018.
2. Y. Chien, J. Wang, and J. Wang. A 0.2 v 32-kb 10t sram with 41 nw standby power for iot applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 65(8):2443–2454, Aug 2018.
3. Hiroshi Fuketa, Masanori Hashimoto, Yukio Mitsuyama, and Takao Onoye. Alpha-particle-induced soft errors and multiple cell upsets in 65-nm 10t subthreshold sram. In 2010 IEEE International Reliability Physics Symposium, pages 213–217. IEEE, 2010.
4. Akhilesh Goyal, Abhishek Tomar, and Aman Goyal. Effect of w/l ratio on sram cell snm for high-speed application. International Re- search Journal of Engineering and Technology (IRJET), 2017.
5. Evelyn Grossar, Michele Stucchi, Karen Maex, and Wim Dehaene. Read stability and write-ability analysis of sram cells for nanome- ter technologies. IEEE Journal of Solid-State Circuits, 41(11):2577– 2588, 2006.
6. Peter Hazucha, T Karnik, J Maiz, S Walstra, B Bloechel, J Tschanz, G Dermer, S Hareland, P Armstrong, and S Borkar. Neutron soft er- ror rate measurements in a 90-nm cmos process and scaling trends in sram from 0.25-/spl mu/m to 90-nm generation. In IEEE Interna- tional Electron Devices Meeting 2003, pages 21–5. IEEE, 2003.

7. Nathan Ickes, Gordon Gammie, Mahmut E Sinangil, Rahul Rithe, Jie Gu, Alice Wang, Hugh Mair, Satyendra Datla, Bing Rong, Sushma Honnavara-Prasad, et al. A 28 nm 0.6 v low power dsp for mobile applications. IEEE Journal of Solid-State Circuits, 47(1):35–46, 2012.
8. Tae Woo Oh, Hanwool Jeong, Kyoman Kang, Juhyun Park, Younghwi Yang, and Seong-Ook Jung. Power-gated 9t sram cell for low-energy operation. IEEE Transactions on Very Large Scale Inte- gration (VLSI) Systems, 25(3):1183–1187, 2017M..
9. Harold Pilo, John Barwin, Geordie Braceras, Christopher Browning, Steve Burns, John Gabric, Steve Lamphier, Mark Miller, Al Roberts, and Fred Towler. An sram design in 65nm and 45nm technology nodes featuring read and write-assist circuits to expand operating voltage. In VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on, pages 15–16. IEEE, 2006.
10. Singh Pooran, Vishvakarma, and Santosh Kumar. Ultra-low power high stability 8t sram for application in object tracking system. IEEE ACCESS, 6:2279–2290, 2018.
11. Kazi Fatima Sharif, Riazul Islam, Mahbubul Haque, Marzia Akhter Keka, and Satyendra N Biswas. 7t sram based memory cell. In Innovative Mechanisms for Industry Applications (ICIMIA), 2017 International Conference on, pages 191–194. IEEE, 2017.
12. Manish Shrivastava and Vimal Kishore Yadav. Low power schmitt trigger based sram using 32nm finfet devices. Materials Today: Proceedings, 5(1):1578–1584, 2018.

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