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Fault Analysis of 3to 8 Decoder implemented using Quantum Dot Cellular Automata for State Configuration

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Abstract ***As the Complementary Metal oxide Semiconductor Field effect transistor has reached its limits of further increase in the device density as Per Moore's law, there are alternate technologies like the Carbon Nano tube Field effect Transistor, Quantum Computing gates, Spintronics, Quantum Dot Cellular Automata(QCA), of which QCA has the advantages of high device density, improvised latency and less power consumption. Hence there is need for design of QCA circuits as well as testing of such circuits for various defects. In this research we have focused on the Fault analysis of a 3 to 8 Decoder constructed using Five input Majority Voter with Coplanar Wire crossing. The Frame work provided is to detect the fault occurring at the QCA configurations and fault injection is performed to estimate the error rate in QCA Circuits.***

Keywords: Quantum Dot Cellular Automata, Struck at Faults, decoder.

I. INTRODUCTION

The Field coupled Nano computing technology like Quantum Dot Cellular Automata (QCA) has gained much momentum after the International Technology Roadmap for Semiconductors (ITRS) has indicated that the predictions of Intel Moore's law leads to new technology by the Year 2020 [1-4]. Quantum dots are made up of four dot Quantum wells which can hold an electron in each its dot and occupies the diagonal spots in a Quantum Dot due to electrostatic force of attraction and repulsion [2-4]. The Quantum cells can represent a stable configuration of Binary value of '0' or '1'[5-6] which can be used for transmitting information through a series of cellular automata. There are various QCA configurations that can be used to accomplish the construction of digital circuits such as QCA wire, Inverter and Majority Voter[7]. Various architectures are developed using QCA technology and works focusing on defect and fault analysis had been done [8-9]. In this work, the focus is on defect tracking in QCA based 3 to 8 decoder constructed using high input majority voter in coplanar wire crossing method [8].

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II. EXISTING DESIGN OF 3 TO 8 DECODER

The Random-Access Memory (RAM) in a configurable logic block (CLB) requires address decoders to identify the Unit memory cell in a loop based LUT . Hence efficient design of decoder is essential for a Parallel Memory architecture. In Fig 1, the circuit diagram of 3 to 8 decoder with enable input and with outputs from OUT 0 to OUT 7 is presented with the truth table which obeys the Boolean expression, for example OUT 0 = EA'B'C' with truth table in table I.

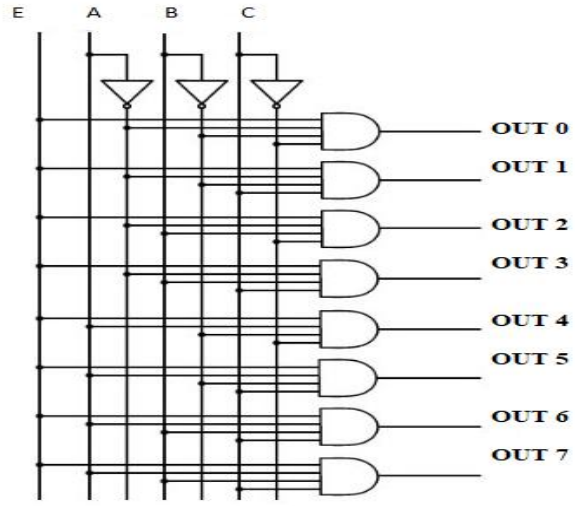


Fig 1 Decoder diagram

The 3 to 8 decoder with enable input has been designed in QCA using five input Majority voter using coplanar wire crossing and Zone based clocking for triggering the cells [8][10].

Table I Truth table

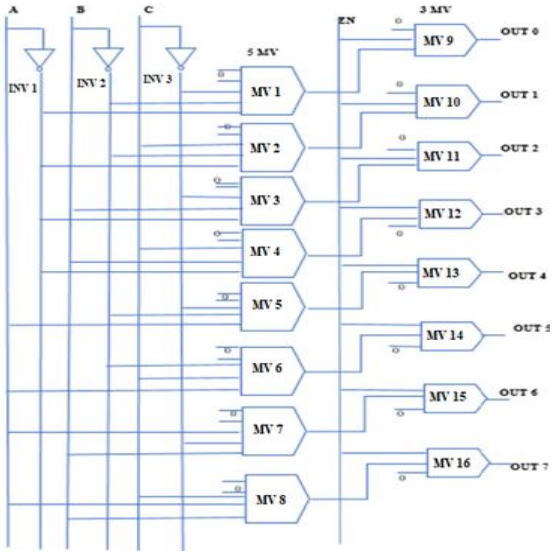
EN	A	B	C	Y= OUT N	Output Expression
1	0	0	0	OUT 0	EA'B'C'
1	0	0	1	OUT 1	EA'B'C
1	0	1	0	OUT 2	EA'BC'
1	0	1	1	OUT 3	EA'BC
1	1	0	0	OUT 4	EAB'C'
1	1	0	1	OUT 5	EAB'C

1	1	1	0	OUT 6	EABC’
1	1	1	1	OUT 7	EABC

The design has to be analyzed for the various faults occurring in the circuit level design using QCA. In general Defects in QCA are classified in to defects in synthesis phase, clock circuitry and deposition phase [11-12].

III.DEFECT ANALYSIS OF 3 TO 8 DECODER

In this work, the focus is to analyze the possibility of faults occurring in the circuit level design as shown in the Fig 2. The faults along the line can occur anywhere between the wires, interconnects, inverters, Majority Voter and in Clocking.



In this work, the paper discusses the Struck at faults due to the inverter, three input and five input majority voter. The inverters are denoted as INV 1,INV 2 and INV 3 and the Majority Voters from MV 1 to MV 16.In the design of the 3 to 8 Reversible Decoder shown in Fig 3., consider the Five input Majority Voter MV1 can be given by the following expression F(MV1) = A’B’C’.

Fig 2 Circuit Level Design of QCA

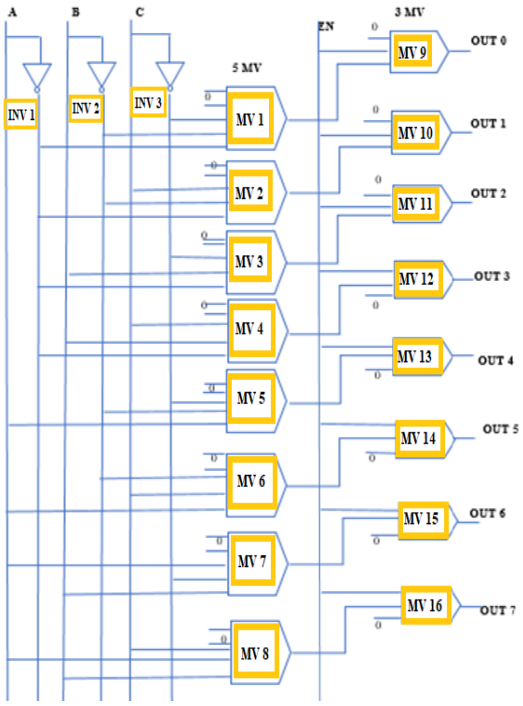


Fig 3 Majority Voter configuration of 3 to 8 Decoder with fault injection

Hence the output Boolean function is implemented by the MV1 depends on the possibility of struck at faults occurring at inverted inputs A, B, C and at MV1. The Boolean function of the MV9 is given by., F (MV9) = OUT 0 = EA’B’C’ - Eq (1) Similarly, for the output functions of the Majority voters of the 3 to 8 decoder can be derived as in Table II. The fault analysis is performed by considering struck at fault induced at inverter, five input and three input majority Voter by considering the Boolean functions in table II. [13-14]The Flow chart of the fault injection and fault analysis is represented in Fig 4. The table III and IV presents the S-a-0 and S-a-1 faults that would occur in the circuit considering the Inverters **INV 1**$_A$, **INV 2**$_B$, **INV 3**$_C$. The State configuration is verified by the output Boolean function indicated in the Table II.

TABLE IIOutput Boolean Function of MajorityVoter

Majority Voter	Boolean Function	Majority Voter	Boolean Function
MV 1	F (MV 1) =A’B’C’	MV 9	F (MV 9) =OUT 0 = EA’B’C’
MV 2	F (MV 2) =A’B’C	MV 10	F (MV 10) =OUT 1 = EA’B’C
MV 3	F (MV 3) =A’BC’	MV 11	F (MV 11) =OUT 2= EA’BC’
MV 4	F (MV 4) =A’BC	MV 12	F (MV 12) =OUT 3 = EA’BC
MV 5	F (MV 5) =AB’C’	MV 13	F (MV 13) =OUT 4 = EAB’C’
MV 6	F (MV 6) =AB’C	MV 14	F (MV 14) =OUT 5 = EAB’C
MV 7	F (MV 7) =ABC’	MV 15	F (MV 15) =OUT 6 = EABC’
MV 8	F (MV 8) =ABC	MV 16	F (MV 16) =OUT 7 = EABC

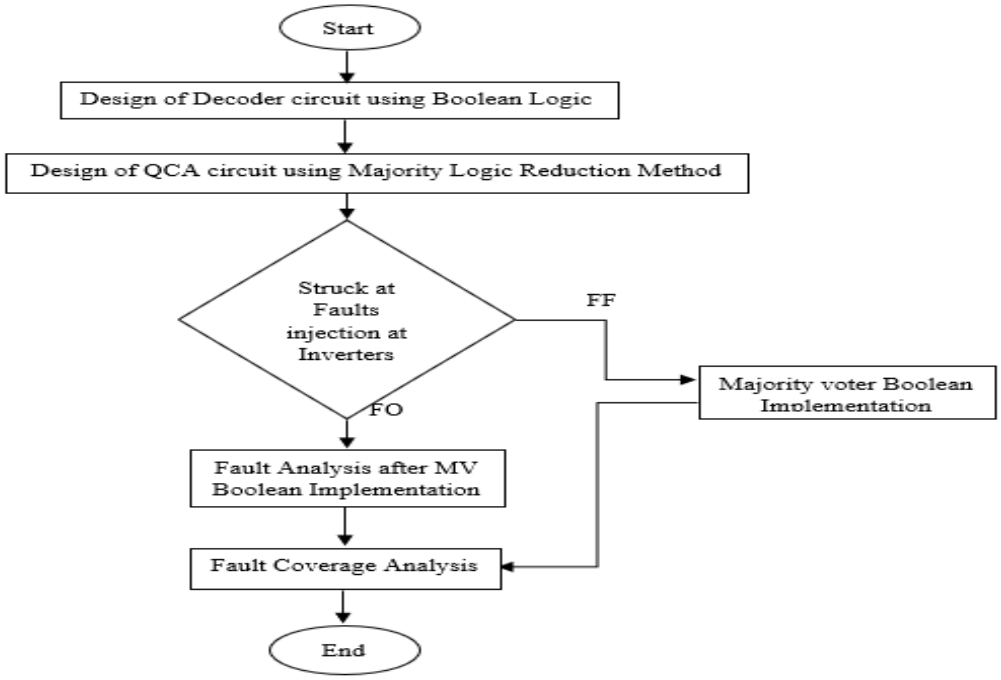


Fig 4 Flow chart for the Fault analysis of 3 to 8 Decoder using QCA

Table III Struck at Faults(s-a-0) at the Inverter configuration

A	B	C	**INV 1_A**	**INV 2_B**	**INV 3_C**	**INV 1_A** (s-a-0)	**INV 2_B** (s-a-0)	**INV 3_C** (s-a-0)	**Majority Voter**	**Final OUT**
0	0	0	1	1	1	0	0	0	F(MV1) = 0	F(MV9) = 0
0	0	1	1	1	0	0	0	0	F(MV2) = 0	F(MV10) = 0
0	1	0	1	0	1	0	0	0	F(MV3) = 0	F(MV11) = 0
0	1	1	1	0	0	0	0	0	F(MV4) = 0	F(MV12) = 0
1	0	0	0	1	1	0	0	0	F(MV5) = 0	F(MV13) = 0
1	0	1	0	1	1	0	0	0	F(MV6) = 0	F(MV14) = 0
1	1	0	0	0	1	0	0	0	F(MV7) = 0	F(MV15) = 0
1	1	1	0	0	0	0	0	0	F(MV8) = 1	F(MV16) = 1

Table IV Struck at Faults at the Inverter configuration

A	B	C	**INV 1_A**	**INV 2_B**	**INV 3_C**	**INV 1_A** (s-a-1)	**INV 2_B** (s-a-1)	**INV 3_C** (s-a-1)	**Majority Voter**	**Final OUT**
0	0	0	1	1	1	1	1	1	F(MV1) = 1	F(MV9) = 1
0	0	1	1	1	0	1	1	1	F(MV2) = 1	F(MV10) = 1
0	1	0	1	0	1	1	1	1	F(MV3) = 1	F(MV11) = 1
0	1	1	1	0	0	1	1	1	F(MV4) = 1	F(MV12) = 1
1	0	0	0	1	1	1	1	1	F(MV5) = 1	F(MV13) = 1
1	0	1	0	1	1	1	1	1	F(MV6) = 1	F(MV14) = 1
1	1	0	0	0	1	1	1	1	F(MV7) = 1	F(MV15) = 1
1	1	1	0	0	0	1	1	1	F(MV8) = 1	F(MV16) = 1

Table V Faulty and Fault Free Outputs

Boolean Function	E/FF	F(MV)/FF	E/FO	F(MV)/FO
F (MV 9) =OUT 0 = E. F(MV1)	1	F(MV1) = 1	0	F(MV1) = 0
F (MV 10) =OUT 1 = E. F(MV2)	1	F(MV2) = 1	0	F(MV2) = 0
F (MV 11) =OUT 2 = E. F(MV3)	1	F(MV3) = 1	0	F(MV3) = 0
F (MV 12) =OUT 3 = E. F(MV4)	1	F(MV4) = 1	0	F(MV4) = 0
F (MV 13) =OUT 4 = E. F(MV5)	1	F(MV5) = 1	0	F(MV5) = 0
F (MV 14) =OUT 5 = E. F(MV6)	1	F(MV6) = 1	0	F(MV6) = 0
F (MV 15) =OUT 6 = E. F(MV7)	1	F(MV7) = 1	0	F(MV7) = 0
F (MV 16) =OUT 7 = E. F(MV8)	1	F(MV8) = 1	0	F(MV8) = 0

In table V, the Faulty and fault free outputs are given. The Scope of the paper is to consider the probability that the struck at faults either s-a-0 or s-a-1 occurs at the invertersand majority voters instead of the individual and joint probability of occurrence of struck at faults, otherwise the complexity of analysis increases furthermore. In Table V, the error analysis between the faulty output and faulty free output gives the complete variation with the desired and expected output.

IV. CONCLUSION

Thus, the present research paper focusses on the fault injection and fault analysis using the frame work designed for struck of faults. The focus is on the testing of state configurations of Inverters and Majority voters. The frame work is efficient in analyzing the delay faults in inverters and majority voters.By analyzing the faults, fault tolerant circuits can be designed in the Future.

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