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Analysis of Various TSPC Based D Flip Flops

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Abstract: ***The world is growing at an ultra fast speed and so is the technology. Today small devices with maximum efficiency and minimum power are in demand and so came the flip flops. They are used in large number of applications ranging from data storage to microprocessors. In this paper, reviews of different models of D flip flop are presented including respective circuits and their description and working. They are based upon the TSPC logic which allows to represent the design of D flip flop with smaller area and lower power consumption as compared to master-slave configuration based D flip flop.***

Index Terms: AVL technique, D flip flop, MTCMOS technique, TSPC logic.

I. INTRODUCTION

Flip-flops are the basic unit for creation for the digital models. Each flip flop perform the storage of one bit, that is a combinational model processes and synchronizes the working at a given clock frequency. Flip flop is always clocked. Flip flop is either negative edge triggered or positive edge triggered which implies that the input affects the output when the clock goes from higher-to-lower or lower-to-higher logic, respectively. There are two types of flip flops on the basis of how it stores the data. The flip flop which stores the data either during the positive edge or during the negative edge of clock signal applied to it are defined as single-edge-triggered flip flops and the flip-flop which save or store the data on both of the positive as well as negative edge of the clock signal applied to the flip flop are termed as dual-edge-triggered flip-flops.

During past years, VLSI designers were more tilted towards the silicon area consumption and its performance. The power dissipation was also one of the parameters. Moreover, cost and reliability also gained dominance. But this scenario is changing at a rapid rate and energy consumption is also given significant preference to that of size and speed of operation. The device performance main issues are- delay in propagation and consumption of power in the circuit. Dissipation of power is one of the main ingredients in any given circuit.

In this paper, review of number of various D flip flops which are based on TSPC dynamic logic like conventional D flip flop based on TSPC logic with 11 transistors, D flip flop based on TSPC logic using 9 transistors, D flip flop based on TSPC logic flip flop incorporating only 5 transistors, D flip flop based on TSPC logic with 5 transistors using MTCMOS and D flip flop based on TSPC logic with 5 transistors AVL technique.

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II. VARIOUS IMPLEMENTATIONS OF D FLIP FLOP BASED ON TSPC LOGIC

Many varieties of D flip flop have been proposed in the past. Various conventional techniques like master-slave configuration and pulsed triggered flip flops have been used as designing methodologies for D flip flop. This paper presents review on different small area dynamic TSPC designs of D flip flop which were proposed in the past. Since, these D flip flops have low transistor count, thus they are compact. Synchronization is established in TSPC fashion of designing by employing only one clock signal and it results in freedom from clock skew problem.

A. 11T TSPC D Flip Flop

The following diagram depicts a D flip flop based on TSPC principle which triggers on the rising edge. It is made up of alternating p-block and n-block and same clock drives all of the flip flops. It consists of 11 transistors in four simple stages.

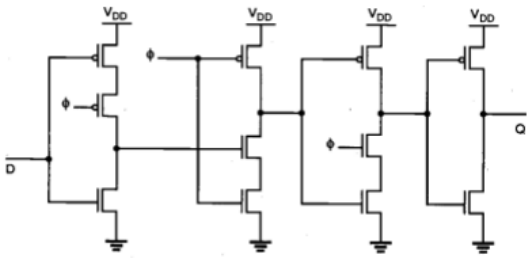

Figure 1 : D flip flop based on TSPC logic with 11 transistors

The first unit pretends as a transparent latch to obtain the input D when the clock is at zero or low level while the output node of the second unit is being pre-charged. The previous output stage is kept by the third and fourth units during that cycle. When the clock signal is high, the first unit denies being transparent and evaluation is started by the second stage. At the same moment, the sampled value is sent to the output of the third stage because it becomes transparent. The non-inverted output level is obtained by the final stage.

B. 9T TSPC D Flip Flop

The figure below shows a D type flip flop based on TSPC principle which is triggered by edge transition of clock.

It consist of 9 transistors which includes four PMOS and five NMOS transistors in three stages, i.e., without the inverting stage of TSPC based Rising Edge Triggered Flip Flop.

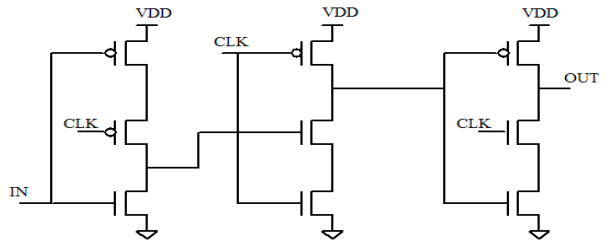

Figure 2 : 9 transistors TSPC based D flip flop

The first unit behaves as a transparent latch to obtain the input D when clock signal resides at lower level logic whereas the output of the next unit gets pre-charged. Previous output stage is kept by the third and fourth units during that cycle. When the clock goes to higher logic level, the first unit denies to be transparent and evaluation is started by the second stage. At the same moment, the third stage becomes transparent and sends the sampled value to the output.

C. D Flip Flop based upon TSPC logic with 5 Transistors

The figure below depicts the circuit of D Flip Flop based on TSPC logic using 5 transistors. It is made up of three NMOS and two PMOS transistors.

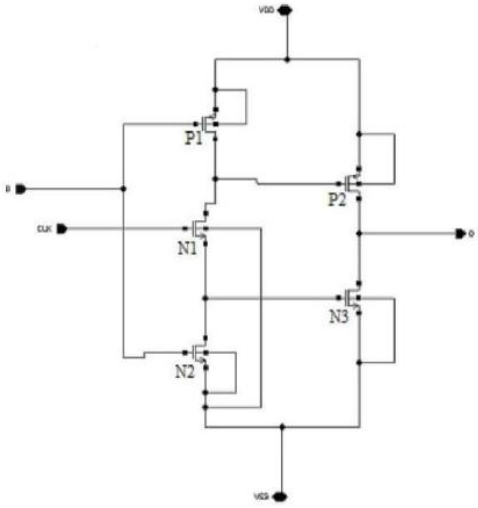

Figure 3 : D flip flop based upon TSPC logic with 5 transistors

Table 1: Truth Table of 5-T TSPC based D flip flop

CLK	D	P1	N1	N2	P2	N3	Q
1	0	ON	ON	OFF	OFF	ON	0
1	1	OFF	ON	ON	ON	OFF	1
0	0	ON	OFF	OFF	OFF	OFF	0
0	1	OFF	OFF	ON	OFF	OFF	0

In short, when Clock signal and D input are high, the transistors PMOS in first stage and NMOS in second stage are inhibited and other transistors are turned on. The high output is obtained. During the period when the clock is active, the circuit transmits the input to output.

D. 5T TSPC D Flip Flop with MTCMOS

The standby current is depreciated by Multi-Threshold Voltage Complimentary Metal Oxide Semiconductor (MTCMOS) by incorporating elevated-threshold voltage devices in series with low threshold voltage circuits. Effectual power management is obtained by sleep governance technique. When the circuit is active, at that time the sleep signal is at low level and consequently inverted sleep signal is at high level, i.e., the transistors are turned on. The source and ground voltages, i.e., VDDV and VSSV executes almost as real power lines due to the on-resistances of the sleep transistors being small. In idle mode, sleep signal is set at high logic, whereas, inverted sleep signal is given low logic, i.e., the sleep transistors are inhibited, and the stand-by current is lowered. This means that in idle mode, the power rails are cut off for reducing the leakage power by turning off the sleep transistors in the circuit. This is the basic working of MTCMOS technique, which is applied in this simulation.

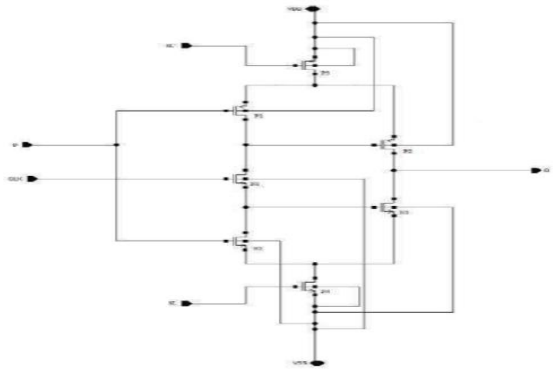

Figure 4: D flip flop based upon TSPC logic of 5 transistors with MTCMOS

The figure above shows the circuit design of D Flip Flop based on TSPC logic of 5 transistors using MTCMOS technique. Two sleep transistors, i.e., one PMOS at source and one NMOS transistor are incorporated in this design. The NMOS sleep transistor is given the signal SL (sleep) and the PMOS sleep transistor is given signal SL' (complement of sleep). Both the sleep and inverted sleep signals are provided with high VTH. When sleep signal is given zero logic and inverted sleep signal is high, at that time in the main circuit with low threshold voltage, there will be zero current flow. On the other hand, sleep signal is high and inverted sleep signal is set with zero logic, then the given circuit implements such that it is in normal mode.

E. 5T TSPC D Flip Flop with AVL Technique

An Adaptive Voltage Level(AVL) technique is often used to control circuits either at the higher end of the circuit design to lower the source voltage value called AVLS method; or at the bottom end of the circuit design to elevate the ground voltage, called AVLG method.

AVL Technique can be introduced in two ways AVLG as well as AVLS technique.

(i) D flip flop based on TSPC logic with 5 transistors using AVLG technique

In AVLG technique, combinations of one NMOS & two PMOS transistors are joined in parallel, such that the input clock signal can be applied to the NMOS transistor of the AVLG network and remaining PMOS transistors are gated with the ground potential.

The AVLG network is attached to the ground end of basic D Flip Flop based on TSPC logic with 5 transistors by removing ground.

Diagram below shows the circuit diagram of D Flip Flop incorporating by AVLG technique.

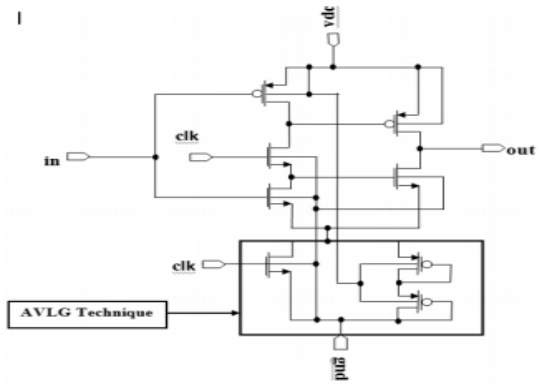

Figure 5: D flip flop based on TSPC logic with 5 transistors using AVLG technique

(ii) D flip flop based on TSPC logic with 5 transistors using AVLS technique

The AVLS scheme uses a parallel combination of one PMOS and two NMOS transistors; such that the clock input is also connected at the PMOS transistor of the AVLS network whereas the remaining two NMOS are gated to drain ends of the respective transistors.

This AVLS network is placed in between the source voltage and basic 5 transistors TSPC D Flip Flop by removing voltage supply source. Diagram below shows the circuit of D- Flip flop by incorporating AVLS technique.

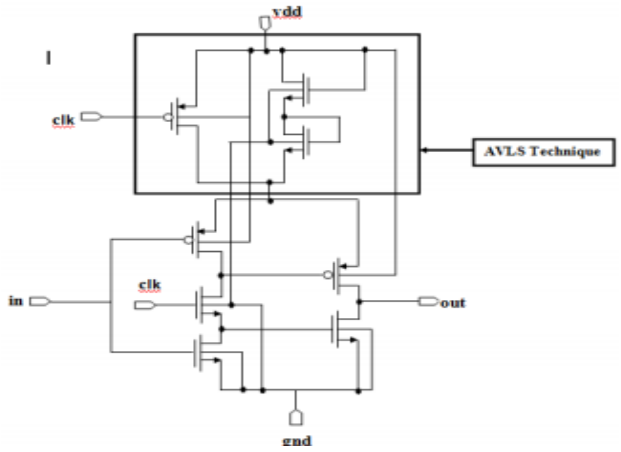

Figure 6: D flip flop based on TSPC logic with 5 transistors using AVLS technique

One of the main advantages of AVL techniques is that it is highly efficient in reducing both the leakage power and the dynamic power. It eliminates the use of variable threshold devices. This approach is highly advantageous for state retention.

But the disadvantage of this method is that it increases propagation delay. Also, the layout area increases.

III. CONCLUSION

On the basis of above stated reviews of different TSPC based D Flip Flop models ,it can be concluded that there is a trade-off between the number of transistors used, i.e., the area consumption with that of the power dissipated by the D flip flop models.

The minimum area is consumed by 5 transistor TSPC based D Flip Flop but it consumes more energy as compared to D Flip Flop using AVLS Technique which consumes the least power among all stated above but occupies more area due to more number of transistors used.

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Anwesha Deb is pursuing her B. Tech in the discipline of Electronics and Communication Engineering from Indira Gandhi Delhi Technical University for Women (IGDTUW). Her area of interest includes Very Large Scale Integration (VLSI) and Digital Electronics.

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