Self-Controlled PFCA Memory Based On Pre Calculation Mechanism

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Abstract : Content-addressable memory (CAM) is every now and again utilized in applications, for example, query tables, databases, cooperative figuring, and systems administration, that require fast inquiries because of its capacity to improve application execution by utilizing parallel correlation with diminish seek time. Despite the fact that the utilization of parallel examination results in diminished pursuit time, it likewise altogether expands control utilization. In this concise, a Pre-calculation based proposed method useful for fast applications. The SCPF engineering is helpful in applications where look time is vital to plan bigger word lengths. The test results demonstrate that PB-SCPF approach can accomplish all things considered 80% in defer decrease and 32% in power decrease. In this proposed methodology able to achieve lower power consumption with the requirement of cell plan.

Index Terms – Content-Addressable Memory (CAM), ML delay, Self-Controlled Precharge-Free CAM.

I. INTRODUCTION

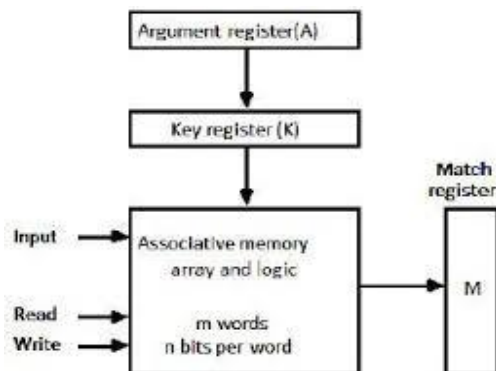Content-addressable memory (CAM) is profitable. It is used in

Fig 1: CAM block

Very high speed application and it consist of argument register and key register and match register. There is a ML (Match Line)

II. EXISTING METHODS

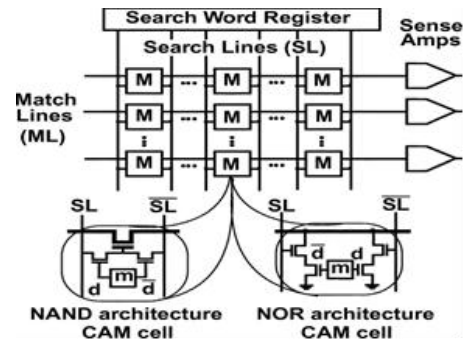In the existing techniques here use NAND type CAM and NOR type CAM.

Fig 2: it shows the simplified structure of CAM along with NAND & NOR CAM architecture

NAND type CAM mainly used for lower consumption of power and NOR type mainly for the better execution. NAND-type CAM cell is for the most part used to lessen the power utilization of the system. In a customary CAM all match-lines (MLs) are to be precharged while before a pursuit. Due to the additional precharge stage it consumers more power and decreases the execution and recurrence of activity.

Limitations: In NAND type ML has to precharge before each search. The speed of hunt task restricted by the precharge cycle and In NOR type power insufficient.

III. PRECHARGE-FREE ML FORMATION

A. Precharge-Free CAM

PF CAM is for the most part proposed to play out the sweep action for greater word lengths. In like manner improve the speed of the movement by remove the PRE stage. In this architecture it consist of 8T CAM.
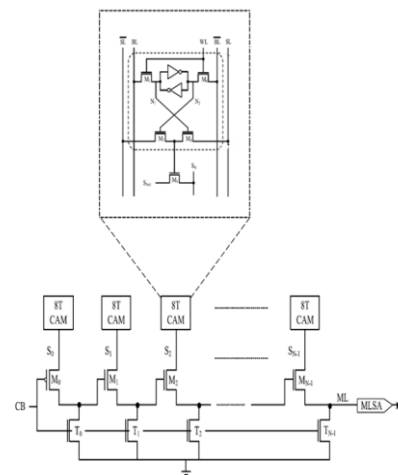

Fig 3. Word Structure of PF CAM

B. Self-Controlled Precharge-Free CAM

In this type an event that the hunt content matches the prestored information, at that point it pass a high incentive through the transistor (NMOS) .Otherwise it passes a low an incentive through the transistor (PMOS) to the ML. From the word design, plainly the base working voltage is constrained to VTHP +2VTHN +VM. The voltage VM is for the most part MLSA

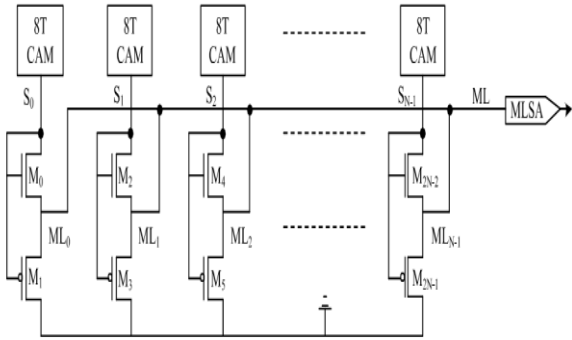Subordinate and the most overwhelming among the three voltages

Fig 4. Word Structure of SCPF-CAM

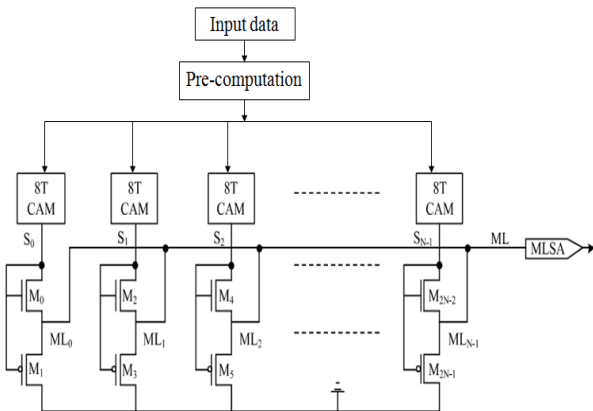### C. Pre-computation Based Self-Controlled Precharge-Free

CAM

Fig. 5 Block Diagram of PB-SCPF CAM

In Pre computation Block, equality bit is presented as parameter for correlation tasks. The equality bit generator is a parameter extractor here that will be utilized for creating equality bit esteem. The upside of utilizing equality as a parameter is that parameter memory is exceedingly diminished correlation with existing frameworks as just a single piece for example k=1 is required for putting away parameter comparing to each put away word whatever might be the length of info information bits. Henceforth, the quantity of examination tasks in pre-calculation is much decreased and subsequently the power utilization of parameter memory. Along these lines, by and large power utilization of the CAM is decreased.

Contrasted and existing strategies, the proposed engineering has improvement in multifaceted nature and territory. The seeking speed is additionally expanded because of decrease in multifaceted nature and decrease in parameter correlation activities. By utilizing equality bits, delay for each inquiry activity is diminished. Thus, it helps the hunt speed of parallel CAM. The number of bits having rationale esteem '1' in a given double information is tallied. In the event that number of bits in the double information is odd, at that point the equality bit esteem is '1' and in the event that the quantity of one's in a twofold information is even, at that point the equality bit esteem is '0'.
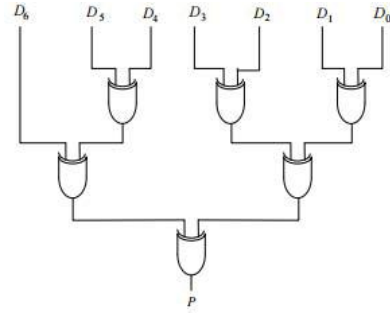
Fig. 6 Logic Circuit of Parity Bit Parameter Extractor

First the parity bit is extracted using parity bit generator and comparisons of extracted parity bit are made with that of stored parity bits. Then, according to the results of parity bit comparisons, a comparison in data memory takes place. Comparisons in data memory will be made only with those stored data words whose corresponding parity bit will be matched with that of input word's parity bit.

IV. RESULT AND PERFORMANCE ANALYSIS

A. Design process

Tanner EDA gives a total line of programming arrangements that catalyze development for the plan, format and check of simple and blended flag incorporated circuits. Clients are making leap forward applications in territories, for example, control the board,
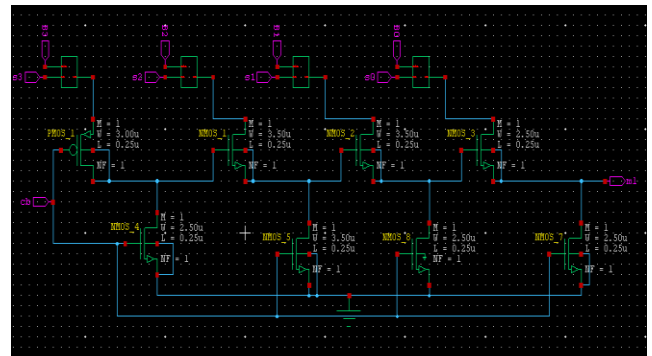
show and imaging, car, buyer gadgets, life sciences, and Radio Frequency (RF) gadgets.
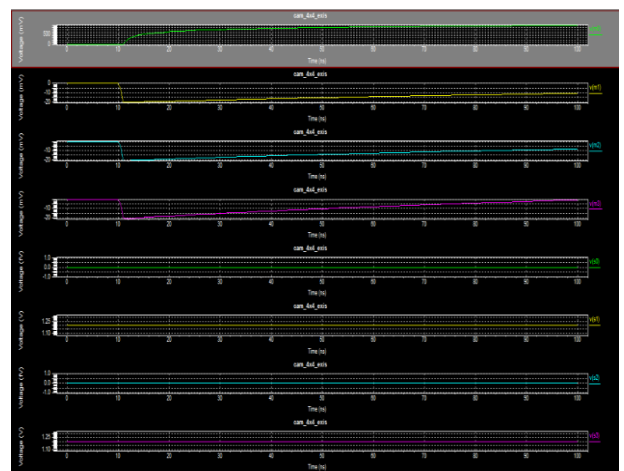
Fig. 7 Design of PF CAM
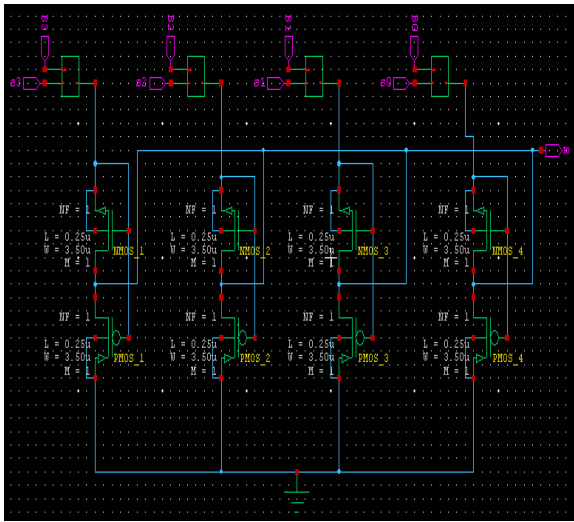
Fig. 8 Output Waveform of PF-CAM
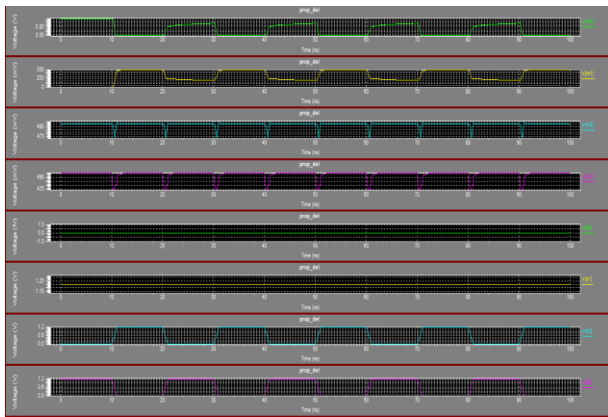
Fig. 9 Design of SCPF CAM

Fig. 10 Output Waveform of SCPF CAM

B. Performance Comparison Summary

The SCPF-CAM produces ML esteem at all time among the thought about structures at the expense of minute extra scattering. With increment in supply voltage, increase in pinnacle control is seen in all the looked at plans. The proposed design it consumes lesser peak power compared to other design.

V. CONCLUSION

The proposed structure is mainly for quick applications, which exhibits the lower ML delay among the separated plans. The proposed course of action keeps up a key detachment from the PRE arrange and overcome the existing limitation. The ML deferral of the proposed plan is 80% of PF-CAM, at the expense of paltry extra scattering. This will be of enthusiasm among planners for shaping bigger word lengths at better inquiry speed.

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