Metal-Oxide-Semiconductor Capacitors Fabricated on Zirconium Oxide High-K Gate Dielectric Nano-Layers

Onkar Mangla, Savita Roy

Abstract— ***In this study, we have fabricated zirconium oxide (ZrO_2) nanolayers on silicon substrates by ablation of ZrO_2 pellet due to interaction with the high temperature, high density and extremely non-equilibrium argon plasma in a modified dense plasma focus device. ZrO_2 nanolayers are fabricated with two bursts of focused plasma on silicon substrates placed at distances of 4.0 cm and 5.0 cm from anode top. The thickness of nanolayers is found to be ~ 30 nm and ~ 20 nm for 4.0 cm and 5.0 cm substrate distances, respectively. Scanning electron microscopy (SEM) studies show formation of uniform nanolayers with nano-size structures of average size ~ 26 nm and ~ 19 nm for 4.0 cm and 5.0 cm substrate distances, respectively. Atomic force microscopy analyses further confirms the size and morphology of nanolayers obtained in SEM results. Current-voltage and capacitance-voltage measurements are done in Al-ZrO_2-Si metal-oxide-semiconductor (MOS) capacitor configuration. Fabricated MOS capacitors have low leakage current density of about 1.72×10^{-8} A/cm^2 at 1 V and capacitance density of about 2.2 μF/cm^2. The conduction mechanisms which governs the electrical properties of MOS capacitors are found to be field/tunnel emission and Schottky emission in low and high electric field regimes, respectively. The fabricated MOS capacitors have improved electrical properties in terms of low leakage current and high capacitance density as compared to others reported in literature which is advantageous for next-generation MOS nanoelectronic devices.***

Keywords: Zirconium oxide; nanolayers; dense plasma focus; metal-oxide-semiconductor; nanoelectronics.

INTRODUCTION

The next-generation nanoelectronic devices require miniaturization of metal-oxide-semiconductor field effect transistors (MOSFETs), which is obtained by reducing the thickness of gate dielectric to sub-100 nm range [1,2]. The gate dielectric which was preferred in MOSFETs is silicon dioxide (SiO_2) before the sub-100 nm technology node. In sub-100 nm technology node SiO2 should be further scale down to have a thickness below 2 nm. The scaling of SiO_2 below 2 nm causes high leakage current and reliability issues such as tunneling [1-3]. In next-generation MOS technology this problem can be alleviate by using materials having high-κ (high dielectric constant) as gate dielectric. High-κ material when used as gate dielectric will results in equivalent capacitance even with physically thicker layer. The high-κ materials used presently as gate dielectric are having several drawbacks like low mobility and interface defect etc. which leads to undesirable carrier scattering [4] and degrade the performance and quality of next-generation MOS devices. Thus, it is necessary to investigate new high-κ material for MOS device technology.

Several high-κ materials such as titanium dioxide [5], tantalum oxide [6], aluminum oxide [7], hafnium oxide (HfO_2) [8], lanthanum oxide (La_2O_3) [9] and ZrO2 [10] have been used as gate dielectric to replace SiO_2. Out of the several high-κ material, HfO_2 is the most explored material for gate dielectric and it also shows improved electrical properties which make it one of the suitable high-κ material for gate dielectric. On the other hand, ZrO_2 is less explored material as gate dielectric but it possess several electrical and structural properties which are superior than HfO2 such as high-κ value of about 26, wide band gap of about 5.7 eV, stable with silicon substrate and gate electrode metals. This makes ZrO_2 more suitable and desirable gate dielectric material than HfO_2. However, the electrical properties of fabricated MOS capacitor are also depends on the method of fabrication of dielectric material.

ZrO_2 thin film for MOS capacitor applications has been deposited by several techniques such as atomic layer deposition [11], e-beam evaporation [12], plasma enhanced chemical vapor deposition [13] and sputtering [14]. Among them plasma based techniques are advantageous because they use ion implantation for deposition. In the similar manner, we have used the modified dense plasma focus (DPF) device making use of high-temperature, high-density and extremely non-equilibrium argon plasma for the ablation of solid target material. The modified DPF device has already been used for deposition of HfO2 [8] and La_2O_3 [9] for MOS capacitor applications.

In this paper, we reported the fabrication of ZrO_2 nanolayers on silicon substrates through material ions generated due to ablation of ZrO_2 pellet by hot, dense and extremely non-equilibrium argon plasma in a modified DPF device. The nanolayers are comprehensively analyzed for their morphological properties using scanning electron microscopy (SEM) and atomic force microscopy (AFM). MOS capacitors fabricated on ZrO_2 nanolayers are analyzed for their electrical properties using current-voltage (J-V) and high frequency capacitance-voltage (C-V) measurements. The obtained results show improvement in MOS nanodevice

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properties and render them a potential candidate for next-generation MOS nanoelectronic technology.

EXPERIMENTAL SETUP

ZrO_2 powder of 5N purity was compressed at a pressure of 10 MPa to form the pellets. These pellets were subsequently sintered for 4h at 800 ºC. These pellets have thickness ~ 5 mm and diameter ~ 13 mm were used as target for deposition and fitted on top of the modified anode of DPF device. RCA cleaned silicon substrates were placed at a distance of 4.0 cm and 5.0 cm from top of the anode. The details of modification in DPF device for nanofabrication and steps for deposition of high-κ materials were reported earlier [8, 9]. ZrO_2 nanolayers were deposited with two bursts of focused argon plasma. SEM images were taken on scanning electron microscope Quanta 200 FEI and atomic force microscope Pico SPM Scan 2100 was used to obtain AFM images. Physical thickness of ZrO_2 nanolayers was measured on SENTECH SE850 laser ellipsometer and is found to be ~ 30 nm and ~ 20 nm for 4.0 cm and 5.0 cm distances, respectively. MOS capacitors were fabricated by making top aluminum electrodes in form of dots through sputtering on as-deposited ZrO_2 nanolayers using shadow mask. The diameter and thickness of top aluminum dots were ~ 200 µm (Area = 31,420 µm2) and ~ 100 nm, respectively. The smooth aluminum film of thickness 200 nm grown by thermal evaporation was used as back-contact for MOS capacitors. J-V and C-V measurements of MOS capacitors were done on semiconductor characterization system KEITHLEY 4200-SCS and Agilent (HP) mode 4284A LCR meter, respectively.

RESULTS AND DISCUSSION

SEM images of ZrO_2 deposited on cleaned silicon substrates which are placed at 4.0 cm and 5.0 cm distances from anode top are shown in Figs. 1 (a) and (b), respectively indicating formation of uniform nanolayers having nano-size structures. The average size of nanostructures found from histogram analysis of SEM image and shown in inset of Figs. 1 (a) and (b) is ~ 26 nm and ~ 19 nm, respectively. It is evident from SEM images that during deposition first a nanolayer of ZrO_2 is formed on the substrate then nano-size structures appeared. The average size of nanostructures is more at 4.0 cm distance as compared to 5.0 cm distance. This is due to the fact that less material ions reaches the substrate when placed at a distance of 5.0 cm because of fountain like trajectory of material ions.

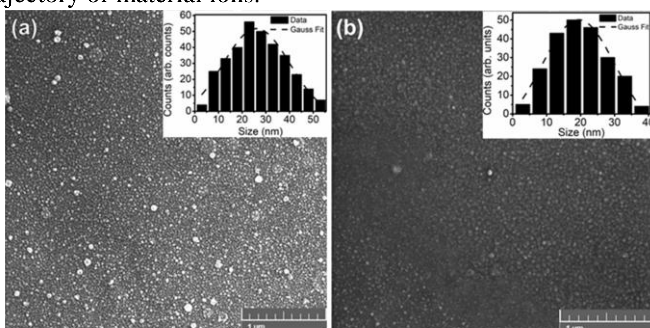

Fig. 1. SEM images and size distributions (in inset) of ZrO_2 nanolayers deposited at (a) 4.0 cm and (b) 5.0 cm substrate distances.

AFM images of samples prepared at 4.0 cm and 5.0 cm distances are shown in Figs. 2 (a) and (b), respectively. Figs. 2 (a) and (b) reveal formation of uniform and continuous nanolayers possessing nanostructures (typical nanostructures shown by arrows have sizes ~ 30 nm and ~ 18 nm, respectively). The quality of fabricated nanolayers is good for the fabrication of MOS capacitors as evident from the low value of root mean square (RMS) roughness found through analysis of AFM images [15]. The value of RMS roughness is ~ 0.13 nm and ~ 0.26 nm for 4.0 cm and 5.0 cm distances, respectively. The RMS roughness of the nanolayers deposited at 4.0 cm distance is less as compared to that deposited at 5.0 cm distance. This suggests that the nanolayers fabricated at 4.0 cm distance are more suitable for MOS nanodevice fabrication.

The analysis of effect of the substrate distance on the electrical properties of the MOS capacitors is done through room-temperature J-V measurements. J-V characteristics of MOS capacitors are shown in Fig. 3 (a) for both the distances. An increase in the leakage current with voltage is observed in J-V characteristics. The value of leakage current for MOS capacitors fabricated on

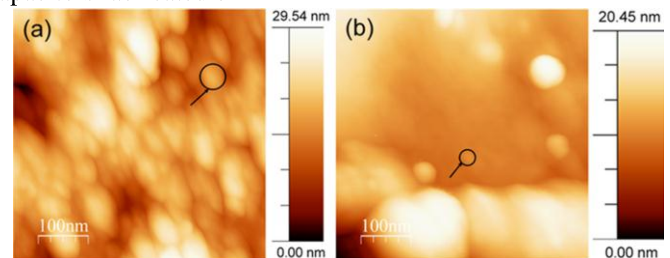

Fig. 2. AFM images of ZrO_2 nanolayers deposited at (a) 4.0 cm and (b) 5.0 cm substrate distances.

ZrO_2 nanolayers formed at 5.0 cm distance is 7.34×10^{-8} A/cm^2 at 1 V, which is more than the value 1.72×10^{-8} A/cm^2 at 1 V obtained for 4.0 cm distance. Moreover, the value of leakage current found in accumulation region is higher in magnitude as compared to that in inversion region for both the distances. This can be due to the differences in properties of material and conduction mechanism at Al/ZrO_2 and ZrO_2/Si interfaces. The value of leakage current obtained in the present experiment is lower than that reported in the literature [13, 16]. J-V characteristics of MOS capacitors fabricated on ZrO_2 nanolayers formed at 4.0 cm distance are further analyzed for finding out the current conduction mechanism. Fig. 3 (b) shows lnJ-$\sqrt{E}$ plot showing near-linear nature having almost same slopes in high field regimes [> 1.5 (MV/cm)$^{1/2}$]. This suggests that the current conduction mechanism involved in present experiment is Schottky emission in high field regimes. On the other hand, the nature of lnJ-$\sqrt{E}$ plot in low field regime [< 1.5 (MV/cm)1/2] has strong dependence on applied voltage, suggesting field/tunnel emission as possible conduction mechanism in this regime [17].Thus, the electrical properties of fabricated MOS capacitors are governed by two current conduction mechanisms namely field/tunnel emission at low field regime and Schottky emission at high field regime.

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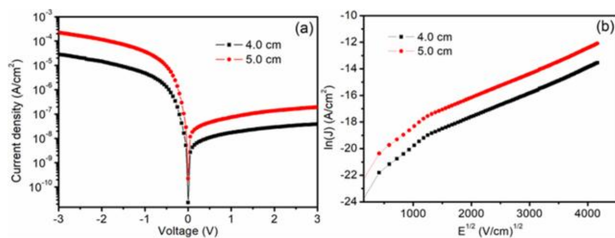

Fig. 3. (a) J-V and (b) ln J-√E characteristics of MOS capacitors fabricated on ZrO_2 nanolayers.

C-V characteristics of MOS capacitors fabricated on ZrO_2 nanolayers formed at 4.0 cm and 5.0 cm distances have measured at high-frequency (1 MHz) and it is shown in Fig. 4. The value of capacitance density is ~ 2.2 $\mu F/cm^2$ for MOS capacitors fabricated on ZrO_2 nanolayers formed at 4.0 cm distance which is higher than the value ~ 1.7 $\mu F/cm^2$ obtained at 5.0 cm distance. It is well known that the capacitance density is lower for thicker films. In the present experiment, the

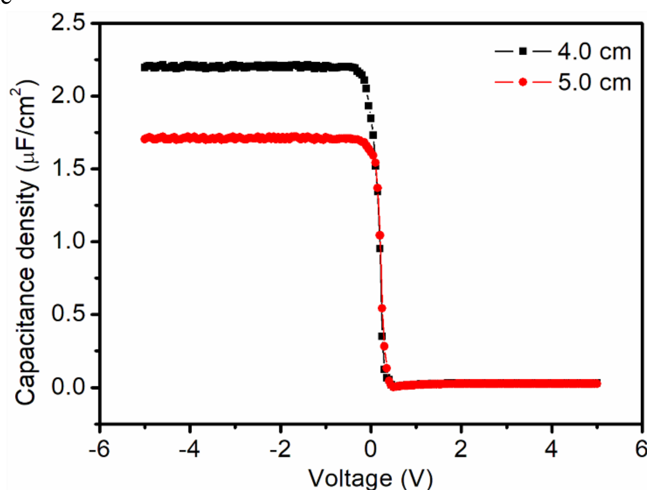

Fig. 4. C-V characteristics of MOS capacitors fabricated on ZrO_2 nanolayers formed at 4.0 cm and 5.0 cm substrate distances.

nanolayer deposited at 4.0 cm distance is thicker than that deposited at 5.0 cm distance, even it has higher capacitance density. This observation may be due to low defects or high crystallinity of the nanolayers formed at 4.0 cm distance. The capacitance densities obtained in present experiment are an order of magnitude higher than that reported in the literature [13, 16]. Thus, the MOS capacitors fabricated in the present experiment on ZrO_2 nanolayers have improved morphological and electrical properties in terms of uniformity, low RMS roughness, low leakage current densities and high capacitance densities. This makes these capacitors a potential candidate for next-generation MOS nanoelectronic technology.

Conclusion

ZrO_2 nanolayers are grown on silicon substrates, placed at a distance of 4.0 cm and 5.0 cm from top of anode, using the ions of ZrO_2 generated by focused argon plasma in a modified DPF device. The nanolayers are found to be uniform containing nano-sized structures. ZrO_2 nanolayers were then integrated into a MOS capacitors. The MOS capacitors fabricated on ZrO_2 nanolayers deposited at 4.0 cm distance have low leakage current density and high capacitance density as compared to that deposited at 5.0 cm distance. It is found that electrical properties of MOS capacitors are governed by field/tunnel emission and schottky emission current conduction mechanisms at low and high field regimes, respectively. The electrical properties of fabricated MOS capacitors are better as compared to earlier reports in term of low leakage current density and high capacitance density. This makes these MOS capacitors a potential candidate for the next-generation CMOS nanodevice applications.

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