Reduction of Power in Sram Cell with Gated VDD Methodology

Aswini Valluri, Muralidharan Jayabalan

ABSTRACT--- Memories are the most important part of portable battery operated digital devices. Since the standard SRAM cells are much power hungry, therefore reducing the power dissipation of memory plays an important role in improving the performance of the system. A low power Static RAM Cell design is analyzed by employing Gated Vdd technique. The outcomes are correlated with the standard 6T, 7T Static RAM cells which show that Gated Vdd technique yields better than the standard 6T and 7T Static RAM cells. The proposed cell dissipates 44.6% lesser power compared to the standard 6T Static RAM cell and 31.09% lesser power to the 7T Static RAM cell. Simulations are performed using Cadence Virtuoso tool with 180nm technology.

Keywords— SRAM(Static Random Access Memory), Power Dissipation, Gated Vdd, 180 nm.

I. INTRODUCTION

In the immense necessity of using cartable devices, battery life plays a significant role. Many advanced devices have been developed where hardware architecture with energy efficiency is necessary. Thus Random Access Memory (RAM) chips are widely inclined in all digital systems. Dynamic Random Access Memory(DRAM)cells requires a periodic refreshing of the power for its function. Whereas Static Random Access Memory(SRAM) cells instead use a persistent power flow for their function. Because of the continuous power SRAM cell need not be refreshed to retain the data being stored. This advantage of SRAM makes it preferred over DRAM.

A standard SRAM cell is designed using 6 Transistors (6T) which is mostly used as its design is very simple [3]. Though its designing is simple, it has a drawback of providing poor stability and also consumes lot of power. Therefore a 6T SRAM Cell [4] with larger Threshold Voltage(Vt) is designed which showed an improvement in stability but degraded the time delay. The limitations have been overcomed in the future design models where the time delay provides perfection but failed in power consumption as it was high [5].This enabled the SRAM cell of using more number of Transistors to achieve a beneficial impact.

A SRAM cell with 7 transistors was designed with low supply voltage which performed well in preventing noise [6]. Different designs of 7T SRAM cells performed well regarding delay, Static Noise Margins(SNMs) and power consumption[7] respectively. Multiple models were designed where 8 to 10 Transistors are used to get better results[8,9,10] in various parameters. In [11], a SRAM cell with 10 Transistors is designed which gained great Static Noise Margin (SNM) and a diminished power of about 20.49%. [12] analyzes a 9T Static RAM cell with stacking and dual threshold voltage for reducing the leakage power. But the drawback with the above designs is the increased area. A new model of 7T SRAM cell was designed which performed well in terms of delay[1], but dissipated more power which can be controlled by employing techniques of power reduction .

In the paper, Gated Vdd technique is used to diminish the power consumed by the Static RAM cell which is correlated with the standard 6T and 7T Static RAM cells .The results were obtained with the help of Cadence Virtuoso in 180nm Technology. The paper is ordered in the succeeding pattern. Section-II represents the standard 6T Static RAM, Section-III explains the working of 7T Static RAM cell, Section-IV describes the proposed Static RAM cell, Section-V gives the results and discussion and thus the paper is wind up with Section-VI.

II. STANDARD 6T SRAM CELL

The construction of a 6T Static RAM cell, capable of storing 1- bit of information is displayed in fig.1 [2]. The entire cell is formed with the help of two cross coupled CMOS inverters, in which the output of one inverter is given as an input to the other one. The feedback loop helps in stabilizing the two inverters to their individual state. The passage transistors M5 and M6, the Word line(WL) and the two bit lines(BL and BL Bar) are used in Writing to the cell or Reading from the cell.

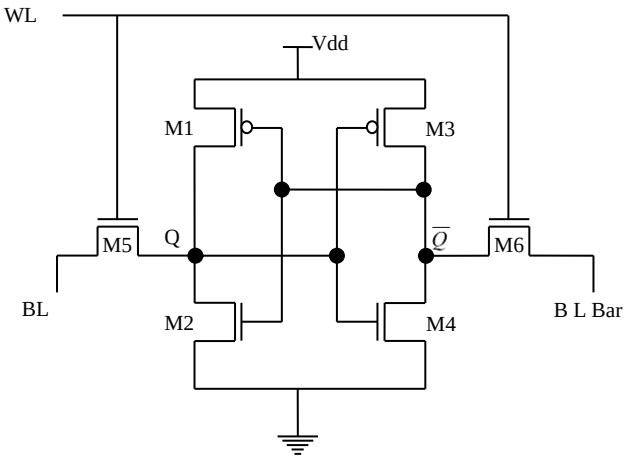

Fig 1: Standard 6T SRAM Cell

Revised Manuscript Received on February 11, 2019.

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To perform a write function, the Word Line is stand to High state i.e to logic1, which enables the passage transistors M5 and M6 by linking the memory cell to the two Bit Lines BL and complement of BL(BL Bar). The value which has to be written is employed to the Bit Lines. Complementary bits are used in order to confirm that the load for charging each of the transistors will be reduced. The values of the two Bit Lines are now shifted to the cell through the passage transistors. For instance, to Write logic1, to the cell, BL is stand to logic1 and BL Bar is stand to logic0. The Word Line is now stand to logic1, permitting the passage transistors to drive the logic value given, from BL and BL Bar into the cell. After successfully completing the Writing operation; the Word Line is stand to logic0.

In order to Read the value present in the cell, Word Line (WL) is charged by logic1. When Word line is high, the two passage transistors starts conducting and connects the inverter inputs and outputs i.e nodes Q and complement of Q to the two Bit Lines BL and complement of BL, respectively. Thus, the two inverters direct the current data value that is stored inside the cell onto the bit lines.

III. 7T SRAM CELL

A 7T Static RAM cell displayed in fig.2[1] uses two PMOS Transistors labeled M1 and M3 and two NMOS Transistors labeled M2 and M4 which are cross coupled to each other to stabilize the inverters to their respective state. Two more NMOS transistors labeled M5 and M6, which act as pass transistors are connected to the nodes Q and $\overline{Q}$ respectively. An additional transistor labeled M7 is connected in correspondence to the M4 transistor whose Gate terminal is given to the RWL(Read Word Line).

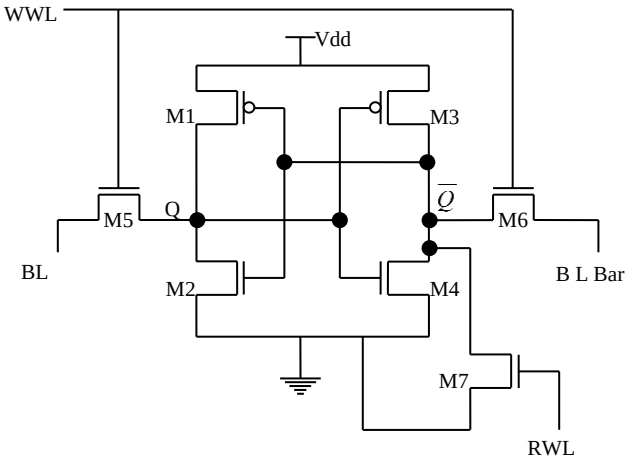

Fig 2: 7T SRAM cell

When WWL (Write Word Line) gets charged, the Write operation will be achieved with the help of access transistors M5 and M6. When RWL(Read Word Line) gets high, the Read operation will be performed. For a Standby state both the RWL and WWL gets discharged by discarding M5, M6 and M7. To perform a write operation; WWL is stand to logic1. To write a logic0 to the cell, BL is stand to the logic0 and BL Bar is stand to logic1.Thus, the storage nodes Q stores logic '0' and $\overline{Q}$ stores logic1. As Q gets a logic0, it will turn ON the transistor M3 and turn OFF the transistor M4. Similarly, as $\overline{Q}$ gets a logic1, it will turn ON the transistor M2 and turn OFF the transistor M1. Thus the access transistor passes the stored logic values from the two bit lines into the cell. To perform a Read operation, RWL (Read Word Line) is stand to logic1 and with use of sense amplifiers, the data is read properly. The design performs better in terms of delay but consumes more power. In order to save the power, different power reduction techniques can be used.

IV. PROPOSED SRAM CELL

The proposed Static RAM cell uses a potent power reduction technique called as Gated Vdd. This technique uses an additional NMOS transistor connected to the ground path as shown in fig.3. The technique instigates a switching mechanism which disables Vdd, the supply voltage, when the Static RAM is not used by terminating the leakage current. Introducing such a transistor helps in reducing the leakage power dissipated by a huge amount. To attain such a mechanism, a transistor of High threshold voltage "High Vt" should be used in the ground path enabling all the remaining transistors to Low threshold voltage "Low Vt". Low Vt Transistors are utilized since they switch quicker than the High Vt Transistors. 'Gated Vdd control' signal is used in order to switch 'ON' or switch 'OFF' the Static RAM cell. Hence the word "Gated" is mentioned to explain such a mechanism. Main benefit of using such a technique is to maintain the system performance though the transistors threshold voltages and supply voltage are diminished.

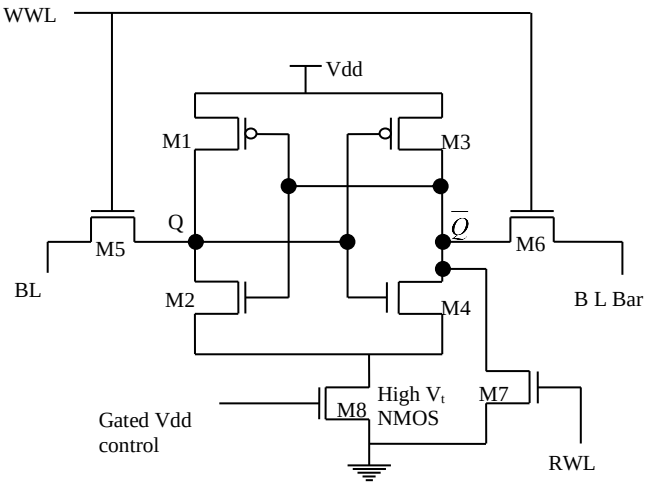

Fig.3: Proposed SRAM cell

V. RESULTS AND DISSCUSSION

The average power dissipation of standard 6T, 7T Static RAM cell and the Gated Vdd Static RAM cell are calculated. Circuit schematics are simulated and designed in 180nm technology with a Vdd of 1.8v using Cadence Virtuoso tool. The average power dissipated by the standard 6T Static RAM cell is 114.3μW, Existing 7T SRAM cell is

91.76µW and for the proposed Gated Vdd, the average power dissipated is 63.23µW as shown in fig.4. The comparison in power savings of 6T, 7T Static RAM cells and the proposed Gated Vdd Static RAM cell is represented in Table – I.

Tbale I Comparision of SRAM Cells

SRAM	AVERAGE POWER (µW)
Standard 6T	114.3
7T	91.76
Proposed	63.23

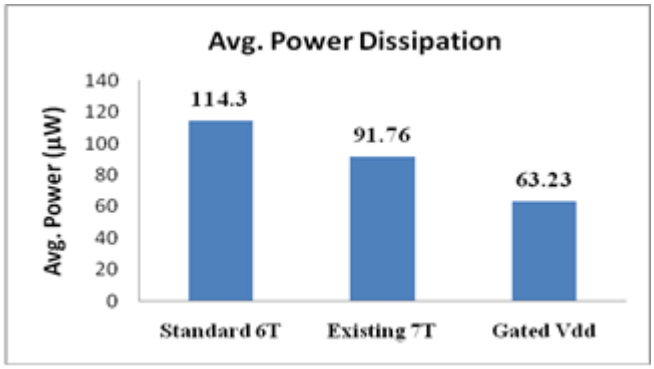

Fig.4: Comparison of Average Power dissipation between various SRAM cells.

It is observed from the above figure that the proposed Gated Vdd Static RAM cell dissipates 31.09% lesser power than the existing 7T Static RAM cell and 44.6% lesser power than the standard 6T Static RAM cell. The proposed Gated Vdd technique dissipates less power, but it should be reminded that the transistor count increases here. This is a trade off for the circuit which dissipates less power. fig. 5 describes the simulation results obtained.

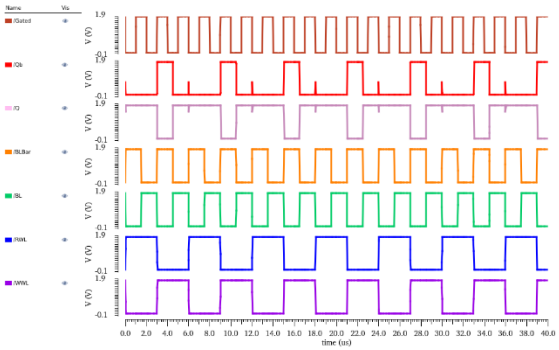

Fig.5: Read and Write operation of Gated Vdd SRAM cell

VI. CONCLUSION

A potent power reduction technique for different SRAM cells is designed named as Gated Vdd in 180nm technology. The Gated Vdd Static RAM cell attains 31.09% power savings compared to the existing 7T Static RAM cell and 44.6% compared to the standard 6T Static RAM cell. After all, in Gated Vdd, the increase of Transistor count in turn affects the area elevated which relates the Trade off with these designs.

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