Design and Analysis of Low Power Full Adder for Portable and Wearable Applications

A. Benjamin Franklin, T. Sasilatha

Abstract--- In this paper, our objective is to design a low power full adder with minimum number of transistors and to analysis the calculated values such as Power, Delay and Power Delay-product (PDP) using 45 nm CMOS process technology. The adder cell is compared with several types widely used adders with different configuration of transistors. The proposed full adder cell has low power consumption, better area efficiency. Designed full adders were evaluated through post-layout Spectre simulations with a 45 nm CMOS technology using Cadence tool. This result shows 20% to 30% improvement in power consumption designed adder that makes it to be used for wide range of applications.

Keywords--- Full Adder, power delay product (PDP) and area, CMOS LOGIC, Low power, Transistor configuration.

I. INTRODUCTION

Brief explanation about the various design procedure for low power VLSI design and it application is presented and a discussion about its impact on upcoming technology growth in the digital world is also presented. Today, power consumption factor plays an important role while designing portable devices and extended battery life for these devices is also a concern that must taken into an account [1].The invention of the electronic transistor caused a large technological leap in electronics. in contrast to the thermionic tube, that needed many hundred volts of anode voltage and few watts of power, the electronic transistor needed only milli-watts of power.

With the advent of the transistor and, decades later, the arrival of the integrated circuit, power dissipation became a lesser concern.

In fact, battery-powered applications drove low-power electronics such as pocket calculators, hearing aids, implantable pacemakers, portable military equipment used by individual soldiers and, most importantly, wristwatches. For all such application, the longer the battery could last, the better. Consequently, ever since then, power requirement reduction has become one of the most critical factors in the evolution of microelectronics technology, even for desktop applications.

To continue to improve the performance of the circuits and to integrate more functions into each chip, feature size had to shrink more and more [2]. As a result, the magnitude of power per unit area has kept growing and the accompanying problem of heat removal and cooling has kept getting worse, as exemplified by general-purpose microprocessors.

Addition is one of the fundamental arithmetic operations and is used extensively in many VLSI systems. In addition to its main task, that is adding 2 binary numbers is the nucleus of the many different applicable operations like subtraction, multiplication, division, address calculation, etc. In most of those systems, the adder component of the important path that determines the performance of the system and therefore the full adder is that the core element of complicated arithmetic circuits.

That's why enhancing the performance of the 1-bit full-adder cell (the building block of the binary adder) is taken into account a major goal.

One of the objectives of this paper is to design a circuit based on 0.18-µm CMOS process technology that can operate at ultralow power supply voltage.

One of the foremost necessary obstacles in decreasing supply voltage is that the giant electronic transistor count and V_{th} loss drawback. This drawback is overcome by designed full adder configuration.

II. REVIEW OF FULL-ADDER DESIGNS

There are standard implementations with various logic styles that have been used in the past to design full-adder cells and these are used for comparison in this paper. Although they all have similar function, the way of producing the intermediate nodes and the outputs, the loads on the inputs and intermediate nodes and the transistor count are varied.

Different logical designs tend to favour one performance aspect at the expense of the others. Few of them use one logical design for the full adder and others can use more than one logic design for their proposed implementation [6].

The complementary pass-transistor logic (CPL), shown in Fig.1 and its truth table in Table-1, with swing restoration, which uses 32 transistors.

CPL produces several intermediate nodes and their complement to form the outputs.

The fundamental distinction between the pass-transistor logic design and also the complementary CMOS logic design is the main aspect of the pass logic electronic transistor network which is connected to some input signals rather than the facility lines [7].

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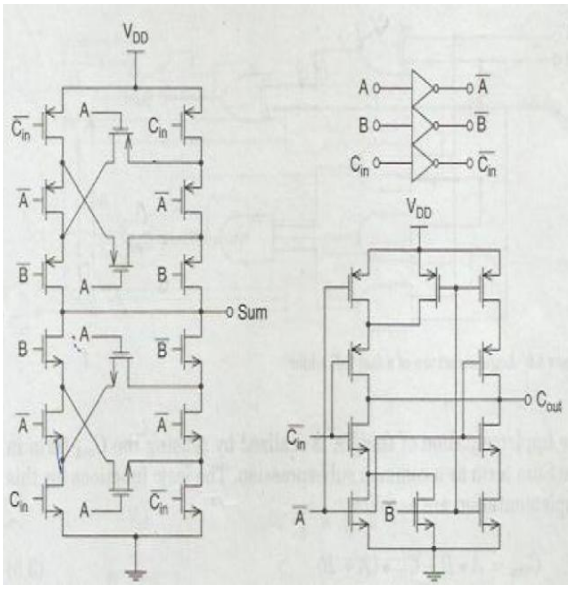

Figure 1: The Conventional CMOS full adder

Table 1: Truth table of a Full Adder

C_{in}	A	B	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

According to Table-1, the logic functions corresponding to terminals Sum and Cout are as follows:

$$\text{Sum} = A \oplus B \oplus Cin \quad (1)$$

$$\text{Cout} = A \cdot B + (A \oplus B) \cdot Cin \quad (2)$$

The pass-transistor network logic is much more capable to implement the logical functions; by that the outputs are generated by a minimumnumber of electronic transistors and a lower input load. Once the transistor gates are oversized the inputs can be overloaded and it may creates high capacitance values. This drawback happens in CPL and CMOS. Pass-transistor logic has an intrinsic problem, which is threshold voltage drop, and output inverters are necessary to guarantee the drivability [3]. CPL could not be a choice for low power aspects because of large transition activity of neighbour nodes, large number of transistors, static inverters and overloading of its inputs.

Another adder, The complementary CMOS full adder (C-CMOS) [1], shown in Fig. 1(a) and its truth table in1(b), is based on a regular CMOS structure with conventional pull-up and pull-down transistors and has 28 transistors. The input capacitance of a static CMOS gate is large because each input is connected to the gate of at least a PMOS and NMOS device. The main use of complementary CMOS logic design is its hardiness against voltage scaling and electronic transistor sizing.

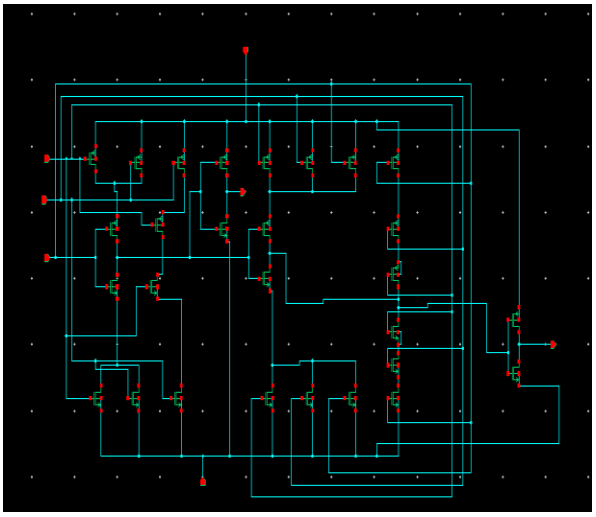

Figure 2: The Complementary CMOS full adder model.

Therefore, to ensure better speed performance, a fast FA has been designed and an alternative implementation of the FA cell that does not OR gates, but instead uses 28 transistors shown in Fig. 2, the implementation of this FA is realized by reusing the Cout term in the Sum term as a common sub expression. The logic functions for this implementation are as follows:

$$\text{Cout} = A \cdot B + Cin \cdot (A + B) \quad (3)$$

$$\text{Sum} = A \cdot B \cdot Cin + (A + B + C) \cdot \overline{Cout} \quad (4)$$

This logic expression deals with realization of full adder without utilization of XOR gate and reusing the Cout term in the Sum term as a common sub expression .This almost reduce 4 transistors from previous adder.

The other two full-adder designs contain transmission function full adder (TFA) [2] (Fig. 3) and transmission gate full adder (TGA) [2] (Fig. 4). These designs are based on transmission function theory and transmission gates and have 17 and 20 transistors, respectively. Transmission gate [5] consists of a PMOS transistor and an NMOS transistor that are connected in parallel way, which is a particular type of pass-transistor logic circuit. The main drawback of this design needs a twice of transistors to design a easier function also, but one of the consideration for use this logic is no voltage drop when implement the design

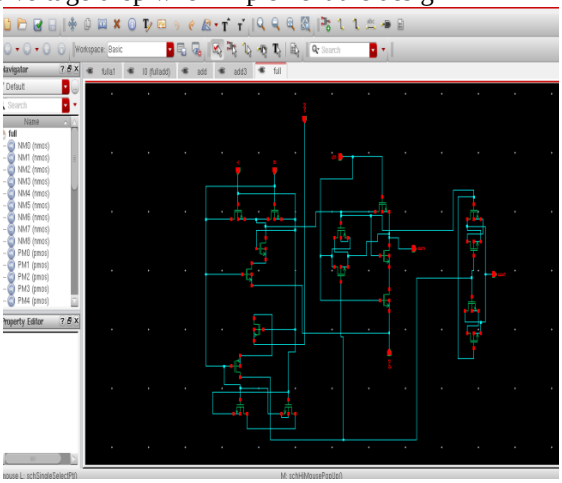

Fig 3: The transmission function full adder (TFA)

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TFA and TGA are inherently low power consuming and they are good for designing XOR or XNOR gates. The main disadvantage of those logic designs is that they reduce the driving capability. Once TGA or TFA are cascaded, their performance degrades considerably [5].

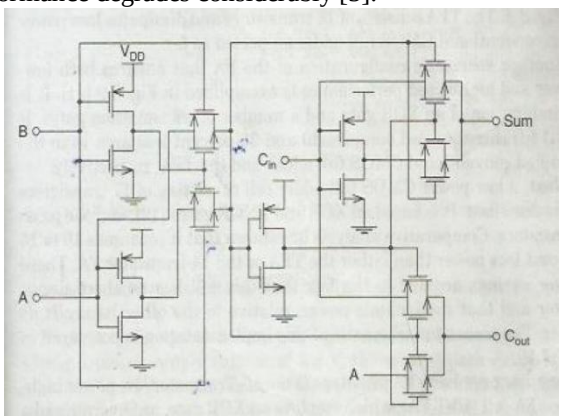

Figure 4: The transmission gate full adder (TGA)

This schematic configuration of the FA that ensures both low-power and high-speed performance is exemplified in Fig. 5. It is a combination of an XOR gate and a number of transmission gates. It has 14 transistors and occupies 30 and 20 percent less area than the 20T Full Adder. CMOS full adder and the TFA, respectively [1].

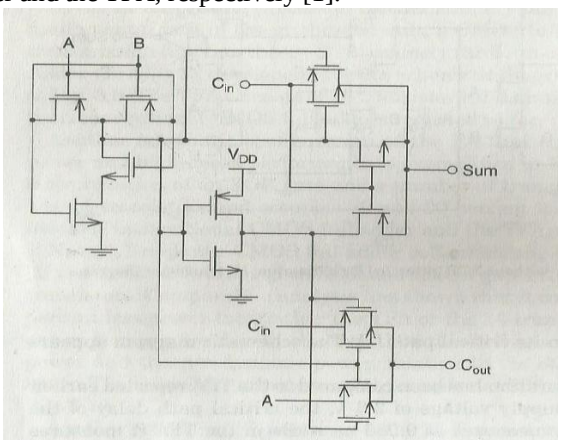

Figure 5: The 14 Transistor Full Adder

Next, a low-power CMOS full adder cell consisting of 17 transistors is described. It is based on XOR and XNOR gates, and the pass-transistors. Comparative analysis has shown that it consumes 10 to 15 percent less power than either the TFA or the 14-transistor FA. These power savings are due to the fact that this cell has no short circuit power and that its dynamic power, relative to the other two cells is lower [4].

III. PROPOSED FULL ADDER DESIGN AND ITS VERIFICATION USING VIRTUOSO

3.1 Static and Dynamic Logic Styles

CMOS logic styles can be categorized into static and dynamic circuits. Static logic families evaluate the out-put whenever there is an input variation, while the dynamic logic gates evaluate the output only once with each clock cycle. In contrast to the static gates design, dynamic gates are clocked and work in the precharge and evaluation phases. Static logic design eliminates the precharging stage and thus reduces the extra power dissipation caused by clocking.

3.2 Proposed Full Adder and it Configuration

The proposed full adder with minimum number of 10 transistors is promising FA prototype with high-speed FA cell (10-T FA) Fig 6,which employs an XOR gate, an inverter and a Pass transistor in its critical path . The schematic diagram appears in figure 6 using virtuoso platform expresses the proposed design. The designed adder is converted from schematic diagram into symbol (Fig 7) for verification and to measurement of both dynamic and static power of the adder.

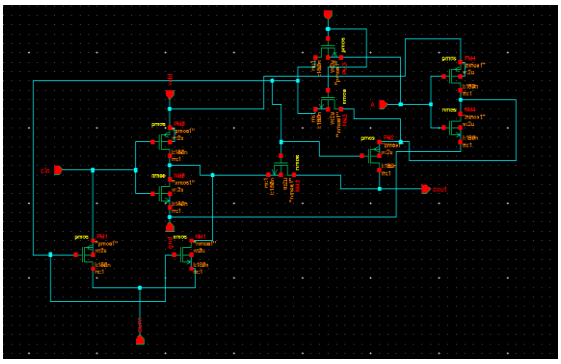

Figure 6: The Proposed 10T Full Adder

This FA configuration has been compared to the TFA reported earlier. Using a power supply voltage of 1.8 V, the critical path delay of the 10-transistor FA measures at 2.18 ns while in the TFA it measures high delay (ns). Also, with the same supply voltage and running a clock frequency of 1GHz, the 10-transistor FA (Fig 6)

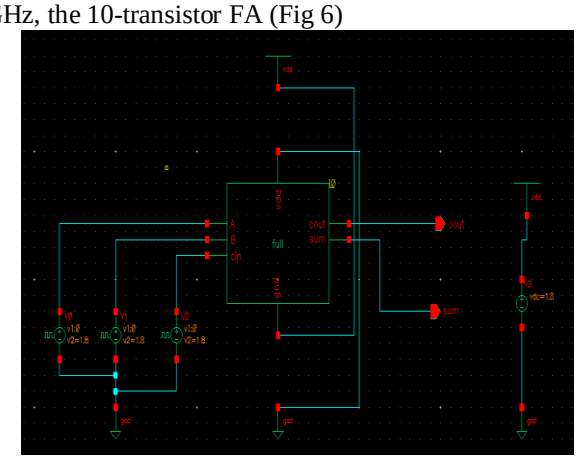

Fig 7: Shows symbol representation of full adder

The procedure followed using virtuoso platform have first step as to set up the suitable parameter to perform the calculation for both dynamic and static by selecting the options such as trans and dc analysis. Dynamic power is nothing but the calculation of power during the transition period of input signal in order to obtain the corresponding output value. Similarly static power represent the ideal or the steady state of input signal without any transfer signal from high to low state or vise versa.

Calculated power values and delay timing has been tabulated (Table 2) in the below section. These values are calculated using the formula editor in the available tool option in the simulation window of virtuoso module.

Table 2: Comparison of power and delay values with varying numbers of transistors.

Number of transistors	Dynamic power(μW) 0V-1.8V	Static power (μW)		Delay(ns)
		0V to 0V	1.8V to1.8V	
32T full adder	253.6 E-6	107 E-6	262 E-6	98.56 ns
28T full adder	83.47 E-6	1.08 E-10	6.64 E-11	54.26 ns
20T full adder	76.56 E-6	1.12 E-10	8.52 E-11	26.59 ns
17T full adder	26.24 E-6	1.04 E-11	3.64 E-11	5.28 ns
14T full adder	1.026 E-3	1.02 E-11	2.82 E-11	4.56 ns
10T full adder	0.978 E-3	8.81 E-12	1.81 E-11	2.18 ns

The graphical modeling of the obtained values has been represented in the below linear graph. The slope clearly shows the deep in the power value (dynamic power) in Fig 8 and with the decrease in power value corresponding to number of transistors.

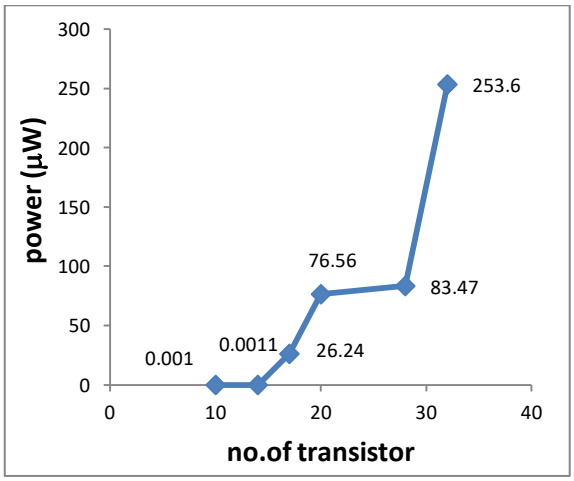

Figure 8: Graphical model of power Vs number of transistors

This representation helps to analysis the result with high accuracy and makes it easy to understand the obtained values.

IV. SIMULATION RESULT AND POST LAYOUT VERIFICATION

The simulated result has been represented in the figure 9, shows how the input signals and output signal are obtained. The list of fields on the right side has the options of choosing power, delay or any other parameter required for analysis. The result obtained is average power and delay with corresponding rise time and fall time at the output signal that is generated.

Figure 9: Simulated result of 10T Full Adder

The proposed 10T full adder must be verified with both pre layout and post layout verification. So the above simulated result shows pre-layout verification for any circuit designed in VLSI technology. Similar to this post layout verification is obtained under the Spectre platform of Cadence tool shown in Fig 10. The basic creation of standard cell design with proper floor planning, placement and routing technique implementation.

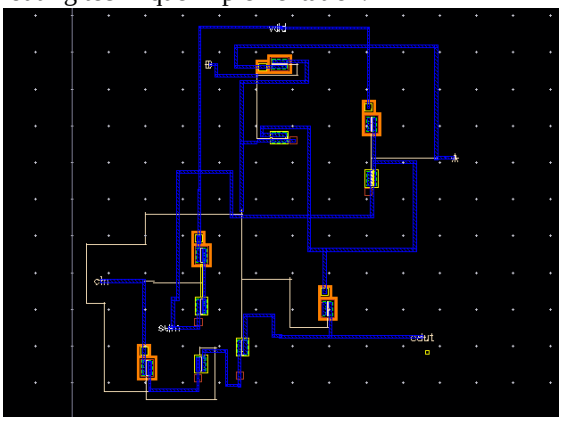

Figure 10: Layout of the 10T Full Adder used in post layout verification

The obtained power value have a increase in its scale after post layout verification as the routing and placement of PMOS and NMOS transistors is done, properties of metal and poly materials used for connection increase resistivity and capacitance of the circuit (Fig 10). The increase in power value due to layout creation is almost 20 % to 30% i.e, the result obtained after post layout of proposed full adder with 10T is almost **1.1736 E-3 (mW)**in dynamic power**.** This value has a impact on the design **after post layout verification** with depends on the various external factors.

V. CONCLUSION

In this paper, a low-power 1-bit full adder has been proposed with minimum number of transistor count. The proposed circuit employs an XOR gate, an inverter and a Pass transistor in its critical path this structure result in a significant reduction in power consumption. Some methodology and techniques has improve the transition and switching speed of the circuitwhich can resulted in the proposed design benefiting from the best PDP and high performance. Simulation have been performed on Cadence environment using a 45 nm technology to evaluate the new design and seven other adders, including 28-transistor complementary CMOS, CPL,TFA,TGA,17T,14Tand lowest power obtained by 10T FA with better area efficiency .Compared simulation results has showed clearly the presented adder is the best PDP. This proposed adder consumes only 20% power higher after layout creation at the post layout verification compared with pre layout phase. The immunity to noise has been also evaluated in this paper. Consequently, this proposed design will be acceptable to be applied for construction of enormous low- power superior VLSI systems and it can work better in the future at higher

technology such as 16nm or 9nm nano-scaling and it is applicable for Portable , wearable and other nano electronics gadgets also.

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