A Simplified Optimal THD Modulation Algorithm for Multi Level Inverter with Reduced Components

V. Karthikeyan, V. Jamuna

Abstract: ***Applications of multi level inverters have been broadly accepted for high power AC drives purposes. In this paper a multi level inverter with reduced number of components has been designed. The power quality of the output waveforms are controlled by proper selection of switching angles for different levels of the output. A simplified optimal THD modulation algorithm is used to calculate the proper switching angles of the output. This algorithm greatly reduces the computational efforts required than the conventional computation methods and also produces better output performances. The simulation model of 9-level asymmetrical inverter with reduced number of components is built to validate its operation and the results are presented.***

Keywords: ***Multi Level Inverter, Reduced Number of Components, Optimal THD Modulation, and Harmonic Distortion.***

I. INTRODUCTION

Now-a-days, the demand for high power equipments has been augmented. High power equipments are typically connected to the medium-voltage network. It is hard to connect a single power semiconductor device directly to the medium-voltage network. For these reasons, a family of Multi Level Inverters (MLIs) has emerged as the solution for high power medium or high voltage applications. It has gained increasing awareness in industry and research since it was introduced in 1980s [1]. A MLI is an array of power semiconductor devices. The advantages of this method over the conventional two-level inverter approach are: improved output power quality, lower voltage stress on the switches and load, improved amplitude of fundamental components and lower electromagnetic interference [2]. The basic function of MLI is to sum up several small DC sources with appropriate switching sequences to the array of power switches so as to obtain a stair-case waveform which resembles the AC sine waveform. Hence inverter action is obtained. The merits of the MLI can be enhanced by increasing the number of steps in the output waveform.

There are three types of basic MLI topologies: Neutral Point Clamped (NPC) [3], Flying Capacitor (FC) [4] and Cascaded H-Bridge (CHB) [5] multi level inverter. Among these topologies CHB multi level inverter (CHBMLI) becomes more trendy, because of its superior reliability arising from its modularity and lesser number of hardware devices. Cascade connection of a number of H-bridge inverters forms a CHBMLI. Each H-bridge inverter can generate three voltage levels in the output. These inverters are classified as: symmetric (each H-bridge is fed by equal DC sources) and asymmetric (each H-bridge is fed by unequal DC sources) MLIs. An asymmetric CHBMLI is preferred to produce more number of output levels with same number of power switches. Conventionally, there are two asymmetrical configurations: binary and ternary. There are various other asymmetrical MLI topologies proposed by many researchers [6]. Since the MLI topologies require reduced voltage stress on the power switching devices, we can realize the high power inverters with low power matured semiconductor technology [7]. MLIs have been used in many applications, such as variable speed AC drives, power quality devices and renewable energy generation such as photovoltaic, wind and fuel cells [8]-[10].

The power quality of the MLI increases as the number of levels in the output increases. The main disadvantage of MLI is the circuit complexity increases, hence the overall cost and size of the system with the increase in the number of levels at the output. To defeat these disadvantages, many topologies are introduced with reduced number of components [11]-[14]. Another major disadvantage with the conventional MLI is the requirement of small isolated DC voltage sources or series bank capacitors. This is overcome by using the renewable energy sources.

The performance of the MLI is mainly depends on the modulation technique used to generate the required gating signals. Different modulation techniques have been introduced to improve the performance of the MLIs [2],[10],[15]-[18]. The commonly used modulation techniques are Selective Harmonic Elimination (SHE) [15], [16], Carrier Based PWM (CBPWM) [17] and Space Vector Modulation (SVM) [18].

In this paper, a Reduced Switch Reverse Voltage (RSRV) multi level inverter with asymmetrical DC sources and reduced number of components is considered. This topology requires lesser number of components than the conventional topologies. The performance of the inverter is controlled by a simplified algorithm of optimal THD modulation for calculating the proper switching angles for different levels of the output. This algorithm reduces the computational complexity of the switching angles of the different levels of output. The operation and performance of the 9-level RSRV-MLI with asymmetrical DC sources are presented and validated through the simulation results.

Manuscript received January 25, 2019.

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II. STRUCTURE OF RSRV-MLI TOPOLOGY

Cascade connection of number of sub-modules forms a Reduced Switch Reverse Voltage (RSRV) MLI topology to produce the required multi level output voltage. The generalized block diagram of asymmetrical RSRV-MLI with reduced components is shown in Figure 1. This topology can be easily extended to higher levels by adding the number of sub-modules. Each sub-module consists of two power switches and one DC voltage source. The switches in one sub-module should not be triggered simultaneously. All the DC voltage sources are asymmetrical and it follows the voltage ratios $1:2^0:2^1:2^2:\ldots:2^{(n-2)}$.

The block diagram shown in Figure 1 consists of two parts, one is magnitude generator or level generator which forms by the cascade connection of number of basic sub-modules (SM) and the other is polarity generator which is the basic H-bridge (HB) circuit. The magnitude generator part is responsible to produce the all possible positive voltage levels (unidirectional staircase waveform) of the output by proper switching function of switches in the magnitude generator part. This unidirectional staircase waveform is applied to the polarity generator part. The polarity generator part provides the alternative polarities to the output of the magnitude generator. So that the alternating output voltage is obtained. The switches in the polarity generator part are operated at the fundamental or line frequency.

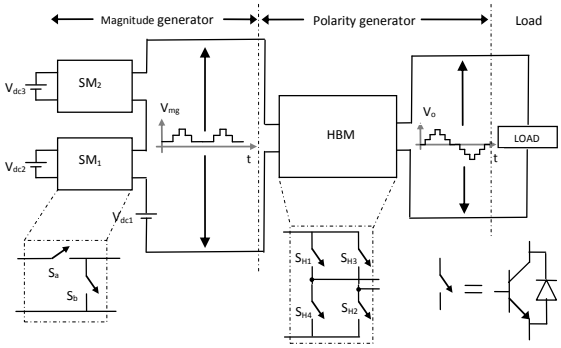

Figure 1: Functional block diagram of the RSRV-MLI

The number of output levels with '*n*' number of asymmetrical sources is given by,

$$N = 2^n + 1 \quad (1)$$

The number of sub-modules (m) required is calculated by,

$$m = n - 1 \quad (2)$$

The maximum output voltage obtainable is given by,

$$V_{o\max} = \frac{(N-1)}{2} \times V_{dc} \quad (3)$$

The number of switches required for this topology with asymmetrical DC sources is given by,

$$N_{sw} \cong \left[\frac{\log(N-1) - 0.301}{0.1505} \right] + 4 \quad (4)$$

The number of driver circuits (N_{dri}) required is equal to the number of switches (N_{sw}) required.

Description of RSRV-MLI Topology

The operation of asymmetrical 9-level RSRV-MLI topology with reduced components is explained with the help of the circuit diagram shown in Figure 2. The circuit diagram of this topology can be divided into two parts, one is magnitude generator part or level generator part other one is polarity part. For 9-level RSRV-MLI, it requires three asymmetrical DC voltage sources (V_{dc1}, V_{dc2}, V_{dc3}), two sub-modules (SM_1, SM_2) and one H-bridge module (HBM). The magnitudes of DC sources are 55V, 55V and 110V.

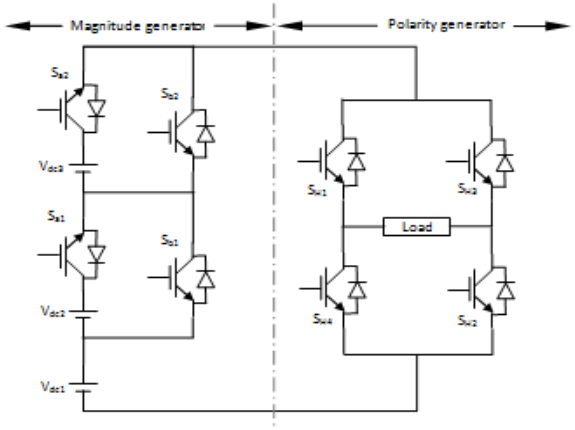

Figure 2: Circuit diagram of 9-level RSRV-MLI

The switches in the magnitude generator parts are operated at the higher frequency (higher than the fundamental frequency) to produce all possible positive output voltage levels by proper switching sequence of switches in the magnitude generator part (S_{ax} and S_{bx}). Here each sub-module contains two power switches. These two switches of each sub-module should not be triggered simultaneously. By proper switching of the switches in the magnitude generator, various possible positive output voltage levels (55V, 110V, 165V and 220V) can be achieved. This produces the unidirectional staircase waveform (V_{mg}). The polarity generator is just an H-bridge module. The function of this polarity generator is to change (reverse) the polarity of the output for every half cycle so that the bidirectional staircase waveform can be achieved. Switches SH_1 & SH_2 are turned ON during positive half cycle, SH_3 & SH_4 are turned ON during negative half cycle and for zero output level, the switches (SH_1 & SH_3) or (SH_2 & SH_4) are turned ON. The switches at polarity generator are operated at the fundamental frequency. Switching sequences of the asymmetrical 9-level RSRV-MLI is given in the Table 1.

Table 1: Switching sequences of 9-level RSRV-MLI

Level	Output Voltage (V_{an})	Switching Functions	
		Magnitude Generator $S_{a1}S_{b1}S_{a2}S_{b2}$	Polarity generator $S_{H1}S_{H2}S_{H3}S_{H4}$
1	$4V_{dc}$	1010	1100
2	$3V_{dc}$	0110	1100
3	$2V_{dc}$	1001	1100
4	V_{dc}	0101	1100
5	0	xxxx	1010/0101
6	$-V_{dc}$	0101	0011
7	$-2V_{dc}$	1001	0011
8	$-3V_{dc}$	0110	0011
9	$-4V_{dc}$	1010	0011

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III. SIMPLIFIED OPTIMAL THD MODULATION ALGORITHM

The performance of the MLI can be enhanced by selecting the proper modulation technique. The simplest modulation technique is the optimal THD modulation which optimizes the total harmonic distortion only and uses the offline switching angle calculation. But the conventional offline switching angle calculation method requires complicated computation techniques like Newton-Raphson method, Resultant theory etc.

The sinusoidal property of the waveform based simplified optimal THD algorithm for calculating the proper switching angles is used in this work. The proper selection of switching angles of MLI produces different voltage levels that lead to a staircase waveform. The property of the sinusoidal waveform is used to determine the appropriate switching angles so that the staircase output waveform resembles to the sinusoidal waveform. This method requires lesser computational efforts as compared to the conventional methods.

These angles for '*N*' (odd numbered) level inverter can be calculated by the following steps,

Step 1: Find the number of switching angles required by,

$$n = \frac{(N-1)}{2} \quad (5)$$

Step 2: The switching angle indexes are,

$$k = 1,2,3,....n \quad (6)$$

Step 3: The switching angles can be calculated by,

$$\sin\alpha(k) = \frac{(k-1)+0.5}{n} \quad (7)$$

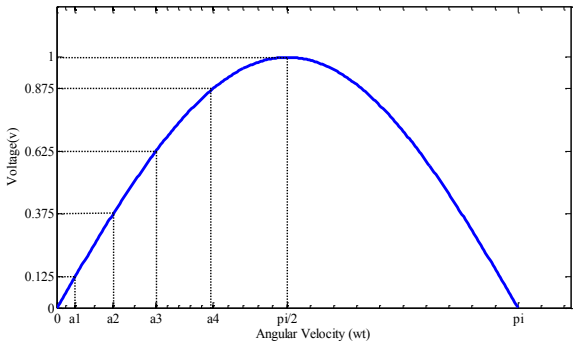

Figure 3 Basic idea of switching angles calculation

The basic idea behind this simplified algorithm is explained with the help of Figure 3. In this, half cycle of sine waveform is considered. For calculating '*k*' number of switching angles, the first half of the half wave is divided into '*k+1*' number of sections by using Equation (7). In Figure 3, switching angle calculation for 9-level inverter is considered. Thus the solutions obtained are given below,

α_1=7.18°, α_2=22.02°, α_3=38.68°, and α_4=61.05°

Thus by providing these switching angles the total harmonic distortion (THD) can be reduced considerably.

IV. RESULTS AND DISCUSSIONS

The feasibility of the RSRV-MLI with simplified optimal THD modulation algorithm, simulations were carried out using MATLAB/Simulink. The developed Simulink model for the proposed topology is shown in Figure 4. For 9-level RSRV-MLI, two sub-modules (SM_1 & SM_2) and one polarity generator module (HBM) were used. The gating pulses for the switches used in the power circuit were generated using the pulse generator block with proper switching angles calculated earlier. The pulses used in polarity generator part and level generator part are shown in Figure 5(a) and 5(b). It is interesting to note that the switches in the polarity generator part are operated at the fundamental frequency and the switches in the level generator part are also operated at lower frequency.

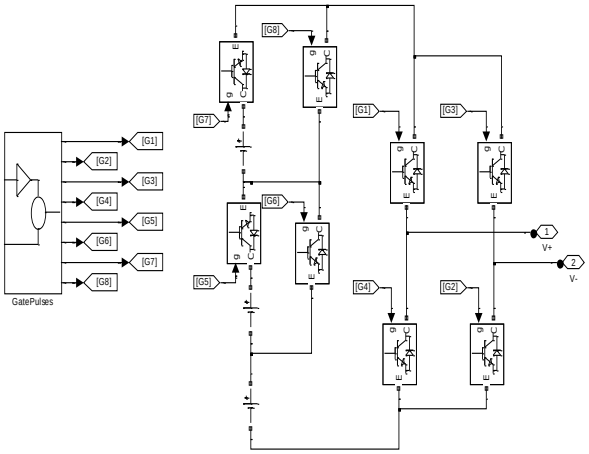

Figure 4: Simulation model of 9-level RSRV-MLI

The output voltage and current waveforms of the 9-level RSRV-MLI with simplified optimal THD modulation and R-load are shown in Figure 6. From the figure, it is clear that the output waveforms contain all the levels as expected and the voltage, current waveforms are in phase. From the harmonic analysis of output waveforms, the fundamental output voltage is 216.5V (peak) and 153.1V (RMS). The voltage and current THDs are 9.34%. Also it contains only the odd harmonics and all the lower order harmonics are lesser than 3%. The harmonic spectrum of the output voltage with R-load is shown in Figure 7.

Table 2: Simulation parameters of 9-level RSRV-MLI

Parameter	Value
Number of levels	9
Number of sub-modules	2
Number of switches	8
Number of DC sources	3 (55V, 55V and 110V)
Modulation	Simplified optimal THD
Switching angles	α_1=7.18°, α_2=22.02°, α_3=38.68°, and α_4=61.05°
Fundamental frequency	50Hz
Load	For R-load 1000Ω, For RL-load 50Ω, 250mH

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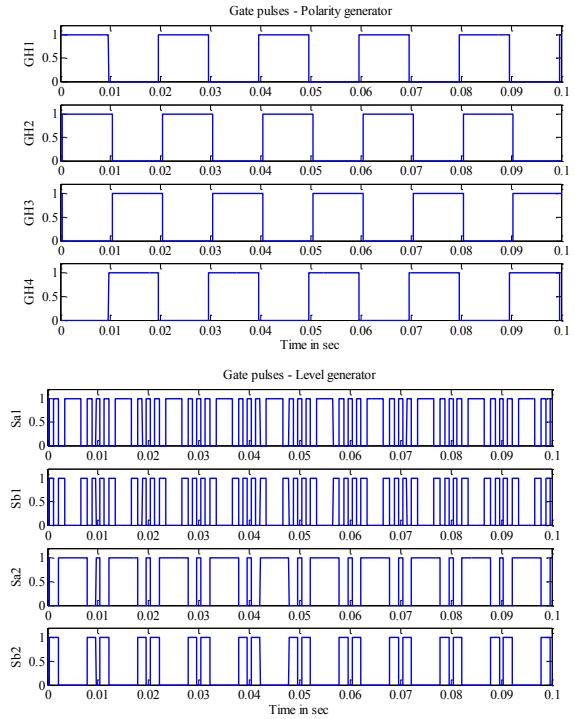


Figure 5: Gating pulses for 9-level RSRV-MLI with simplified optimal THD modulation

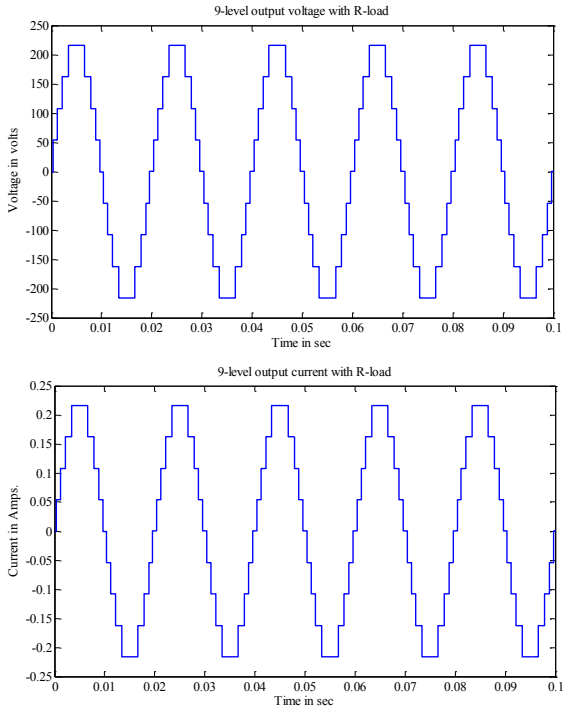


Figure 6: Output voltage and current waveforms of 9-level RSRV-MLI with R-load

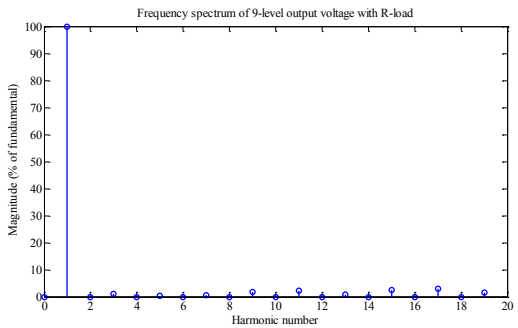


Figure 7: Harmonic spectrum of output voltage and current of 9-level RSRV-MLI with R-load

The output voltage and current waveforms with RL-load is shown in Figure 8. The output voltage waveform contains all the possible nine levels in the output, whereas the output current is smooth sine wave as the load is an inductive nature. From the harmonic analysis of these waveforms, the voltage and current THDs are 9.28% and 0.7% respectively. The peak value of fundamental output voltage and current are 216.3V and 2.324A respectively. The output voltage and current spectrums contains only odd numbered harmonics and there is no even harmonics. Also all the lower order harmonics are having the magnitude lesser than 3% only. The harmonic spectrums of output voltage and current waveforms with RL-load are shown in Figure 9.

The performance of the 9-level RSRV-MLI with simplified optimal THD modulation is compared with single pulse width modulation and summarized in Table 3. From the Table, it is clear that the performance of the simplified optimal THD modulation is very attractive.

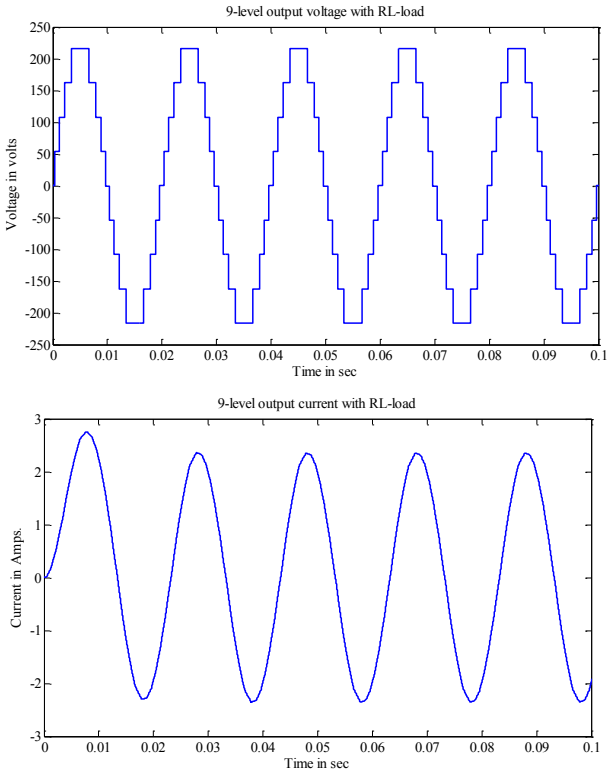
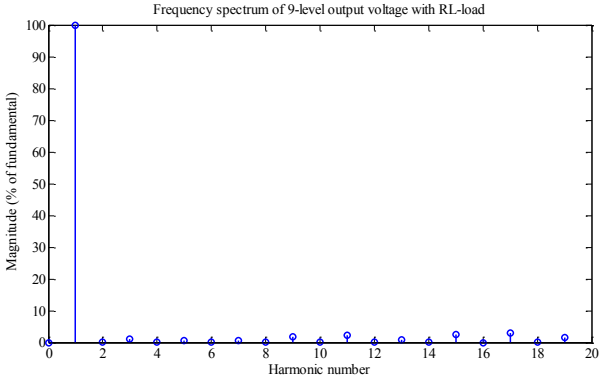


Figure 8: Output voltage and current waveforms of 9-level RSRV-MLI with RL-load



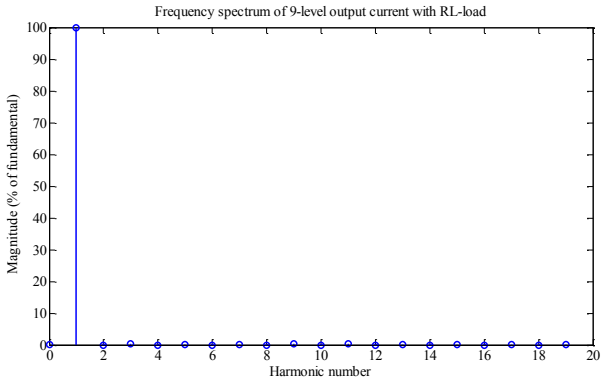


Figure 9: Harmonic spectrum of output voltage and current of 9-level RSRV-MLI with RL-load

Table 3: Performance summary of 9-level RSRV-MLI

Parameter	Single PWM	Simplified optimal THD modulation	
	R-load	R-load	RL-load
Number of levels	9	9	9
Number of switches	8	8	8
Magnitude of fundamental voltage	160.9V	219 V	218.9 V
Magnitude of V_3 (% of fundamental)	25.29	1.05	1.04
Magnitude of V_5 (% of fundamental)	2.47	0.43	0.48
Magnitude of V_7 (% of fundamental)	7.74	0.64	0.66
Magnitude of V_9 (% of fundamental)	1.76	1.89	1.86
Voltage THD (in %)	29.4	9.34	9.33
Current THD (in %)	29.4	9.34	0.7
Distortion Factor (DF)	0.0853	0.0054	0.0054

V. CONCLUSIONS

In this paper, a 9-level asymmetrical RSRV multi level inverter topology with reduced number of components was successfully developed. This inverter requires lesser number of switches when it is used for higher levels. A simplified optimal THD modulation algorithm is demonstrated which is used to calculate the proper switching angles for different levels in the output of the multi level inverter. This greatly reduces the computational efforts required to calculate the same. The presented inverter topology with simplified optimal THD modulation needed lesser number of components, could promise better performance, efficiency, reliability and reduction in size and cost of the inverter. The performances of the 9-level RSRV-MLI with simplified optimal THD modulation are demonstrated with the simulation results.

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