Design of Non-isolated integrated type AC-DC converter with extended voltage gain and high power factor for Class-C&D applications

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Abstract*: *In this paper, an integrated buck-boost buck (IB³) AC-DC converter is proposed with an extended voltage conversion ratio for the class-C&D applications. The proposed converter process the power from input to output in a single stage. This converter is an integration of traditional buck-boost converter and a buck converter shared by a common switch. To get unity input power factor the input buck-boost converter is designed to operate always in discontinuous conduction mode (DCM). The output buck converter is operated in continuous conduction mode (CCM). The necessary design equations have derived using theoretical analysis under steady-state conditions. The features of IB³ converter are fast and tightly regulated dc voltage with extensive voltage gain, unity input power factor and well suit for class-C&D applications with universal voltage range. The proposed IB³ converter is simulated using MATLAB/SIMULINK software to support the theoretical analysis.

Index Terms*: *ac-dc converter, buck-boost buck, integrated converter, power factor correction (PFC), extended voltage gain.

I. INTRODUCTION

Nowadays, a lot of research is going on ac-dc converters, because of their applications. To achieve unity power factor with less harmonic distortion (%THD), and to meet the international standards (IEC 61000-3-2) the power factor correction (PFC) system is needed. The features of PFC system are, enhanced PF, low input %THD, and tightly regulated output. With the PFC system, the traditional ac-dc converters contain of two stages, first stage is the PFC stage and the second stage is the DC-DC regulator stage [1]–[3]. Frequently, boost and buck–boost are preferred for PFC system because of their PFC capabilities when they are operating in discontinuous conduction mode (DCM). These ac-dc converters have two switches hence two separate control techniques are required, which increase the price and complexity of the converter. Because of two power processing units and two switches, the traditional two stage converters fail to produce high efficiencies [4]. To overcome the difficulties, single-stage single switch integrated converters have been developed [5], by integrating a DC-DC regulator with the PFC converter by a common switch. A

number of single-stage PFC based ac-dc converters have been proposed [6-12] with single switch through a simple control. Generally, in single stage converters switch voltage stresses are reliant on bus capacitor voltage. Because of the unregulated bus capacitor voltage, single-stage converters undergo high voltage stresses on the switch. So, bulky capacitors with high rated switching devices are required which increases the cost and limit the applications. Also affects the efficiency of the converter. Besides, these configurations are not suitable to produce wide range outputs, because of restricted voltage gain. The active switch usage of these converters is very poor with low duty ratios [13]. This paper proposes a new buck-boost buck type ac-dc converter to produce the voltage conversion range with excellent PFC characteristics. In addition, the proposed converter has less switch voltage stresses. Integrating or cascading two dc/dc converters can give quadratic function of duty ratio [14] which means extended conversion range. The proposed configuration is an integration of traditional buck-boost converter and a buck converter shared by a common switch for fast and well regulated dc outputs. As a result, a high voltage conversion ratio can be accomplished. So the proposed converter is found to be more suitable for low class-C&D applications compared with conventional ac-dc type converters. To get unity input power factor the input buck-boost converter is designed to operate always in discontinuous conduction mode (DCM). The output buck converter is operated in continuous conduction mode (CCM). The merits of non-isolated IB^3 converter are
1. Unity input power factor.
2. Tightly regulated output with wide voltage conversion.
3. Higher efficiencies.
4. Lower capacitor voltage lead to lower switching stresses.

II. PROPOSED IB^3 CONVERTER

A. Circuit configuration

Figure 1 shows the circuit diagram of the non-isolated IB^3 converter. The buck-boost converter placed at input side includes D_1, L_r, C_r and a switch S, and the buck converter at output includes L_0, D_2, D_F, C_0 and switch S. The value of inductor L_r is chosen to operate i_{Lr} (current through L_r) in DCM so that the average line current is proportional to input line voltage. This makes the input power factor unity as shown on Figure 4.

Retrieval Number: E2079017519/19©BEIESP
Journal Website: www.ijrte.org

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Published By:
Blue Eyes Intelligence Engineering
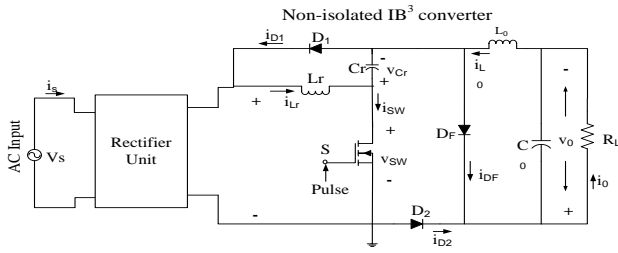*& Sciences Publication*

Fig. 1: Proposed single switch non-isolated Buck-Boost Buck (IB^3) converter

B. Steady-state operation

The operation of the proposed non-isolated IB^3 converter is divided into three modes for a given switching period (T$_s$ = 1/f$_s$) as shown in Figure 2.

Mode-I [t$_0$, t$_1$]: Prior to this interval, the current i_{Lr} is zero, the diode D$_1$ is in reverse biased condition. In mode-I the switch S is turned on at t = t$_0$, the current i$_{Lr}$ linearly increases from zero. Switch S carries load current i$_0$ and i$_{Lr}$. The diodes D$_1$ and D$_F$ continue in reversed biased and D$_2$ is forward biased. Figure 2(a) shows the operation of Mode-I along with the current directions.
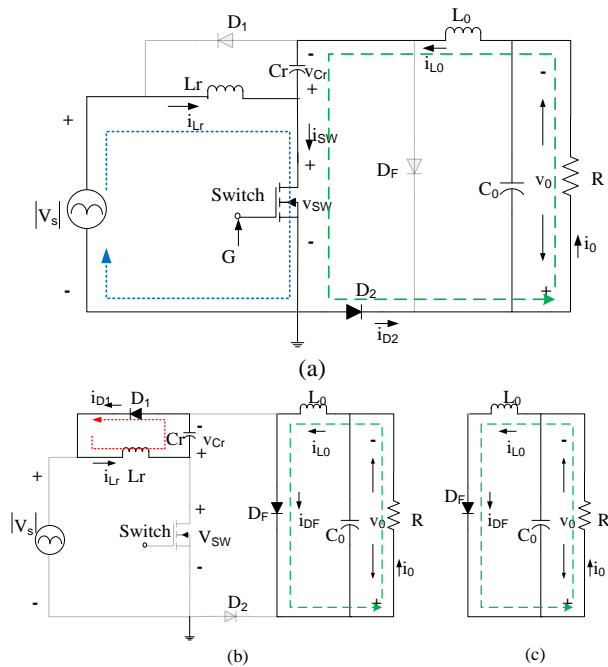

(a)

(b)   (c)

Fig. 2: Steady-state operating modes of IB^3 converter (a) Mode-1 (b) Mode-2 (c) Mode-3

Mode-II [t$_1$, t$_2$]: The switch S is turned off at t$_1$, so the current i_{Lr} discharges through the capacitor C$_r$ transferring the energy to the capacitor. Diode D$_2$ will be reversed biased. The output inductor L$_0$ delivers the energy to the load via diode D$_F$ as shown in Figure 2(b). This mode of operation will continue up to the current i_{Lr} reaches the zero.

Mode-III [t$_2$, t$_3$]: During this mode the current i_{Lr} is at zero whereas current i_{L0} decreases continuously delivering its energy to the load. The converter remains in this mode until the switch is turned on again. This mode of operation is shown in Figure 2(c).

The steady-state operating waveforms for the non-isolated IB^3 converter are shown in Figure 3 for one switching cycle.
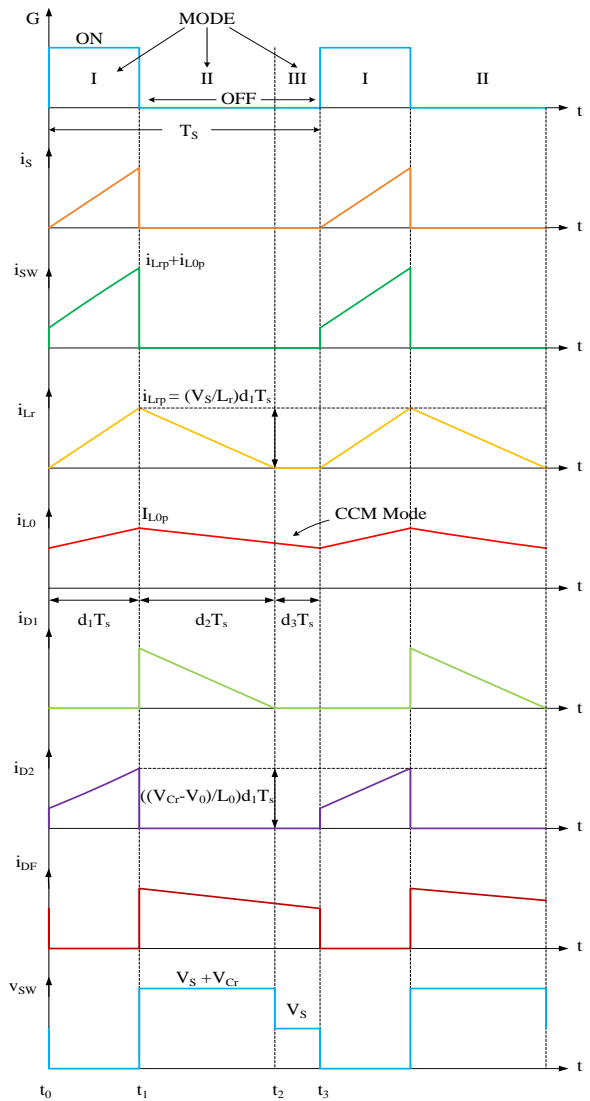

Fig. 3: Steady-state waveforms of proposed single stage PFC Buck-Boost-Buck converter

III. ANALYSIS OF NON-ISOLATED IB^3 CONVERTER

The supply voltage (v$_s$) is sinusoidal is given as $v_s = V_S sin\omega_L t$. The rectified input voltage modulates the line current, as shown in Figure 4. In one switching cycle T$_s$, the input voltage v_s is assumed as constant since the switching frequency f$_s$ (=1/T$_s$) is very high compared with the line frequency f$_L$. The voltage given at the input to the buck-boost buck converter is the rectified ac voltage. Because of this reason the input current pulses have the shape shown in Figure 4. Hence, the input current at a line frequency is given as [1]:

$$\langle i_s \rangle = \frac{i_{sp}}{2T_s} d_1 T_s = \frac{d_1{}^2 V_S}{2L_r f_s} |sin\omega_L t| \qquad (1)$$

where $\langle i_s \rangle$ is input current at time t, i_{sp} is the peak current of each current pulse, V_S is the peak of the supply voltage.

Both input voltage and current waveforms are sinusoidal in shape and in phase, so input power P$_s$ can be written using equation (1) as

$$P_s = \frac{1}{2}V_s \langle i_{sp} \rangle = \frac{d_1^2 V_s^2}{4L_r f_s} \qquad (2)$$

For the given R load, the output power is given as

$$P_0 = \frac{V_0^2}{R} \qquad (3)$$

where V_0 is average output dc voltage. Consider lossless converter, using Equations (2) & (3), the average output voltage V_0 can be obtained as

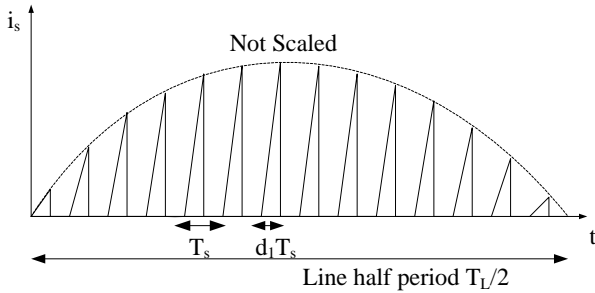$$V_0 = \frac{d_1 V_s}{2}\sqrt{\frac{R}{L_r f_s}} \qquad (4)$$

Fig. 4: Modulated input current pulses with input voltage

IV. DESIGN ANALYSIS

The design analysis of the proposed converter elements L_r, C_r, and L_0 are derived in this section. The output filter capacitor C_0 is chosen to ensure the ripple for the given output voltage. Filter capacitor C_0 will not participate in the circuit dynamics. The dynamics of the non-isolated IB[3] converter with R load is given by

$$L_r \frac{di_{Lr}}{dt} = \begin{cases} |v_s| & for[t_0, t_1] \\ -v_{Cr} & for[t_1, t_2] \\ 0 & for[t_2, t_3] \end{cases}$$

$$C_r \frac{dv_{Cr}}{dt} = \begin{cases} -i_{L0} & for[t_0, t_1] \\ i_{Lr} & for[t_1, t_2] \\ 0 & for[t_2, t_3] \end{cases} \qquad (5)$$

$$L_0 \frac{di_{L0}}{dt} = \begin{cases} v_{Cr} - v_0 & for[t_0, t_1] \\ -v_0 & for[t_1, t_2] \\ -v_0 & for[t_2, t_3] \end{cases}$$

The instantaneous values i_{Lr}, i_{L0} and v_{Cr} given in Equation (5) are averaged over one switching cycle and are represented by I_{Lr}, I_{L0} and V_{Cr}. The rate of change of I_{Lr} in the duration t_0 to t_1 (=T_{on}) is V_s/L_r and the corresponding value in the interval t_1 to t_2 (=T_2) is given by V_{Cr}/L_r. As a result, the average rate of change of I_{Lr} in a switching cycle (T_s) is given as

$$\frac{d}{dt}I_{Lr} = \frac{T_{on}}{T_s L_r}V_s - \frac{T_2}{T_s L_r}V_{Cr} \qquad (6)$$

Similarly for I_{L0} and V_{Cr} over a switching period are given as

$$\frac{d}{dt}I_{L0} = \frac{-R}{L_0}I_{L0} + \frac{T_{on}}{T_s L_0}V_{Cr}$$

$$\frac{d}{dt}V_{Cr} = \frac{T_2}{(T_{on} + T_2)C_r}I_{Lr} - \frac{T_{on}}{T_s C_r}I_{Lo} \qquad (7)$$

The Equations (6) & (7) are represented in state space form is given by

$$\begin{bmatrix} \frac{d\langle I_{Lr} \rangle}{dt} \\ \frac{d\langle I_{L0} \rangle}{dt} \\ \frac{d\langle V_{Cr} \rangle}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{d_2}{L_r} \\ 0 & -\frac{R}{L_0} & \frac{d_1}{L_0} \\ \frac{d_2}{(d_1 + d_2)C_r} & -\frac{d_1}{C_r} & 0 \end{bmatrix} \begin{bmatrix} \langle I_{Lr} \rangle \\ \langle I_{L0} \rangle \\ \langle V_{Cr} \rangle \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{d_1}{L_r} \\ 0 \\ 0 \end{bmatrix} |v_s| \qquad (8)$$

where d_1=$(t_1$-$t_0)/T_s$ and d_2=$(t_2$-$t_1)/T_s$

The input voltage V_s is the rectified value of the input voltage which is constant over a switching cycle. To compute the circuit parameters values V_s is considered. Operating the input inductor L_r in DCM, the average current equation can be obtained as

$$\langle I_{Lr} \rangle = \frac{i_{sp}}{2}(d_1 + d_2) \qquad (9)$$

$$i_{sp} = \frac{V_s}{L_r}(d_1 T_s) \qquad (10)$$

Using Equation (2), input inductance L_r of the proposed converter can be written as

$$L_r = \frac{d_1^2 V_s^2}{4P_0 f_s} \qquad (11)$$

From Equations (3) & (11) the duty ratio d_1 can be obtained as

$$d_1 = \frac{\sqrt{4L_r f_s P_0}}{V_s} = \frac{V_0}{V_s}\sqrt{\frac{4L_r f_s}{R}} \qquad (12)$$

To calculate intermediate bus capacitor C_r value, voltage ripple of the capacitor (ΔV_{Cr}) has to be determined. Low-frequency peak-to-peak capacitor voltage ripple (ΔV_{Cr}) can be obtained using capacitor reactance X_{Cr} as

$$\Delta V_{Cr} = \langle i_{D1} \rangle_{acp} X_{Cr} = \frac{\langle i_{D1} \rangle_{acp}}{2\pi . f_L C_r} \qquad (13)$$

where $\langle i_{D1} \rangle_{ac\,p}$ is the average modulated ac current peak value. Similar to the Equation (1), diode average modulated current $\langle i_{D1} \rangle$ for double the line frequency is given by

$$\langle i_{D1} \rangle = \frac{i_{D1p}}{2T_s}d_2 T_s = \frac{d_1 d_2 V_s}{2L_r f_s}(sin\omega_L t) \qquad (14)$$

Applying volt-sec principle at L_r (using Figure 3) equations is obtained as

$$\frac{v_s}{L_r}d_1 T_s - \frac{V_{Cr}}{L_r}d_2 T_s = 0$$

$$d_1 = d_2 \frac{V_{Cr}}{v_s} \qquad (15)$$

Using Equation (15) in (14), the average modulated diode current $\langle i_{D1} \rangle$ can be obtained by

$$\langle i_{D1} \rangle = \frac{d_1{}^2 V_s{}^2}{2L_r f_s V_{Cr}} (sin^2 \omega_L t)$$

$$= \frac{d_1{}^2 V_s{}^2}{2L_r f_s V_{Cr}} \left(\frac{1 - cos2\omega_L t}{2} \right) \qquad (16)$$

From Equation (16) the low-frequency ac current circulating through storage capacitor C_r and diode D_1 is

$$\langle i_{D1} \rangle_{accontent} = \frac{d_1{}^2 V_s{}^2 cos2\omega_L t}{4L_r f_s V_{Cr}}$$

$$= \langle i_{D1} \rangle_{acp} . cos2\omega_L t \qquad (17)$$

Using Equations (17) & (13), the bus capacitor voltage ripple (ΔV_{Cr}) is derived as

$$\Delta V_{Cr} = \frac{d_1{}^2 V_s{}^2}{8\pi L_r f_s f_L V_{Cr}} \frac{1}{C_r} \qquad (18)$$

So the intermediate bus capacitance C_r, for a considerable voltage ripple (ΔV_{Cr}) is obtained as

$$C_r = \frac{d_1{}^2 V_s{}^2}{8\pi L_r f_s f_L V_{Cr} \Delta V_{Cr}} \qquad (19)$$

The value of output inductance L_0 operating in CCM with a considerable current ripple Δi_{L0} is obtained as

$$L_0 = \frac{(V_{Cr} - V_0) d_1 T_s}{\Delta i_{L0}} \qquad (20)$$

From Equation (19) the capacitor voltage V_{Cr} is inversely proportional to C_r. Hence small values of bus capacitor C_r results in large capacitor voltage V_{Cr} for a given output. This type of selection leads to higher voltage stresses and losses in the switching devices. Higher rating devices will also be needed, which adds to the cost and size. Therefore there is a tradeoff between small size capacitor and the capacitor voltage V_{Cr} of converter. So from the design analysis one thing has to be noted that, to design the converter parameters one of the variables has to be fixed among L_r, L_0, d_1, and C_r. Because, 4 unknowns are governed 3 independent equations as shown in (8). Intermediate bus capacitor voltage V_{Cr} and its ripple ΔV_{Cr} are carefully selected while designing because switching voltage stresses on S, D_1, D_2 and D_F are dependent on bus capacitor voltage V_{Cr}.

The input inductor L_r of the proposed non-isolated converter is operating in DCM mode. So the voltage conversion ratio cannot be the as in CCM mode ($M(d_1) = \frac{d_1{}^2}{(1-d_1)}$). Figure 5 shows the conversion ratio's of different converters. The proposed converter covers more region then the other conventional converters. Another feature is, proposed converter can buck and/or boost the voltages as like the other buck-boost family converters. Proposed non-isolated buck-boost buck converter is capable to produce very low outputs where the buck converter cannot (see figure 5).

Using equation (12) the voltage conversion ratio $M(d_1)$ for the proposed non-isolated converter operating L_r in DCM, can be determined as

$$M(D) = \frac{d_1}{\sqrt{2k}} \qquad (21)$$

The factor k is given by
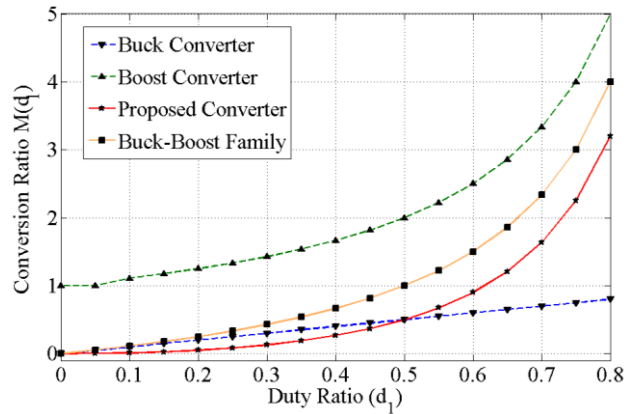
$$k = \frac{2L_r f_s}{R} \qquad (22)$$

**Fig. 5: Comparison of voltage conversion ratio's for different converters**

TABLE-I DESIGNED VALUES OF THE PROPOSED CONVERTER

| Component	Simulation values
L_r	2.25mH
C_r	5uF
L_0	50mH
C_0	1000uF
R Load	250Ω
Converter Input Voltage	84 V_p
Input Line Frequency (f_L)	50 Hz
Switching Frequency (fs)	10 kHz

V. RESULTS & DISCUSSION

The proposed non-isolated IB[3] converter is simulated with MATLAB/SIMULINK software. The calculated element values with input and output specifications are given in table I. These circuit values are calculated based on the design analysis made in previous section. Inductor L_r value is calculated to operate i_{Lr} in the discontinuous conduction mode (DCM) and the inductor L_0 value is chosen to operate current i_{L0} in continuous conduction mode (CCM).

Figure 6 shows simulation waveforms of input current and supply voltage at 0.25 duty ratio. Figure 6(a) represents that the unity power factor with sinusoidally varying current pulses. The zoomed portion shows that the supply voltage is constant for a switching cycle as described in the theoretical analysis. With input LC filter, the converter has produced high input power factor (0.9887) close to unity (Figure 6(b)). Figure 6(c) shows the FFT analysis of the input current at 25% duty ratio. The total harmonic distortion (%THD) of input line current is very less (2.34%) which is under the international standard (IEC 61000-3-2) limits.Figure 7 shows simulated waveforms of input current and supply voltage at 60% duty ratio. Figure 7 proves that the proposed converter produced unity input power factor is for both with & without input filter. Figure 7(c) shows the FFT analysis of the input line current. The %THD of the line current is 1.72%, satisfies the international standards (IEC 61000-3-2).
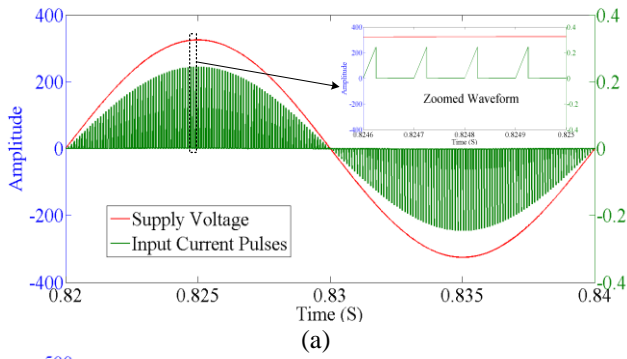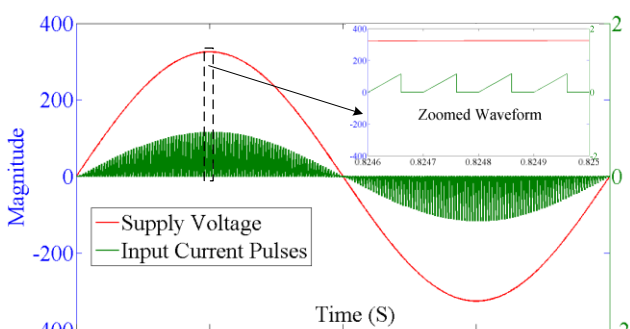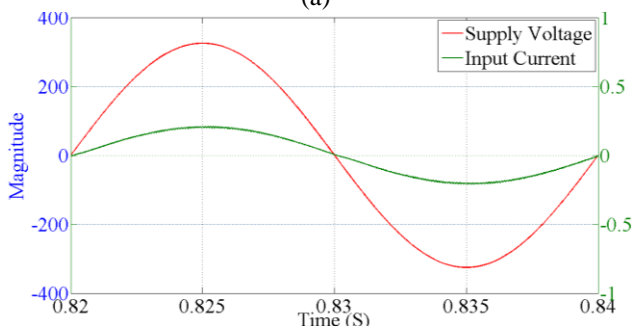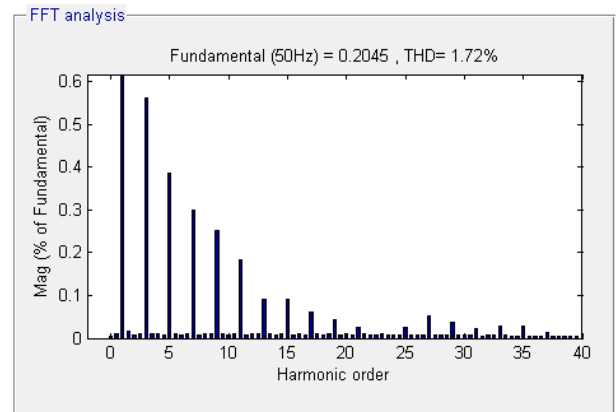
(a)
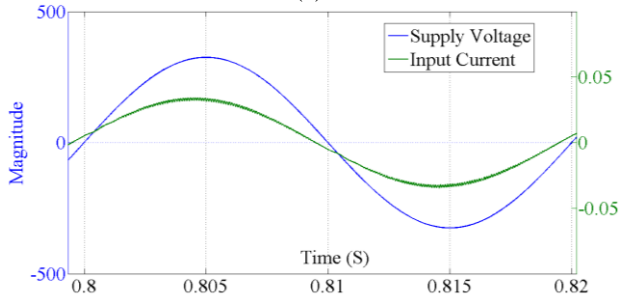
(b)
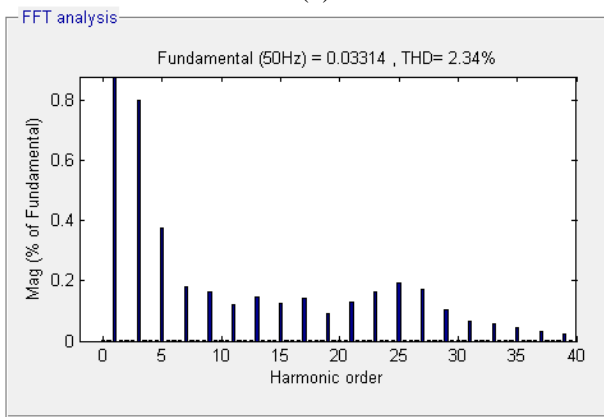
(c)

Fig. 6: Input current and supply voltage: (a) without filter (b) with input LC filter (c) FFT analysis of input current

(a)

(b)

(c)

Fig. 7: Input current and supply voltage at d_1 = 0.60: (a) without filter (b) with filter (c) FFT analysis of input current
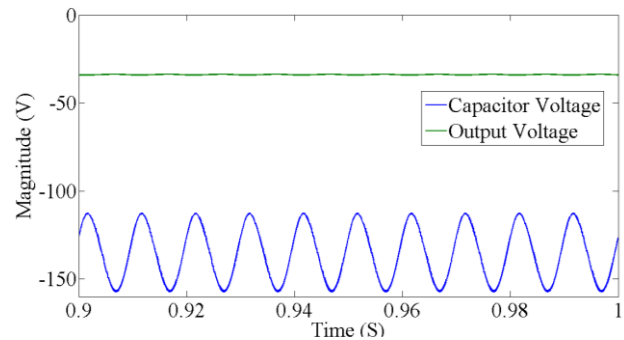

Fig. 8: Capacitor voltage and output voltage at d_1=0.25

Figure 8 represents the bus capacitor voltage V_{Cr} and output voltage V_0 at 25% duty ratio. The non-isolated converter produced 33.2 V inverted average dc voltage with an approximate peak-to-peak ripple of 0.46 V (= 1.4%). This value is fairly same as that calculated using equation (4). The bus capacitor ripple frequency is twice the line frequency (100Hz).

Figure 9 shows the simulated waveforms of the converter operating in steady-state. The waveforms obtained through simulation are same as the theoretical waveforms shown in Figure 3. Figure 9(a) shows the inductor currents i_{Lr} and i_{L0} and 9(b) represents the switch current & voltage.
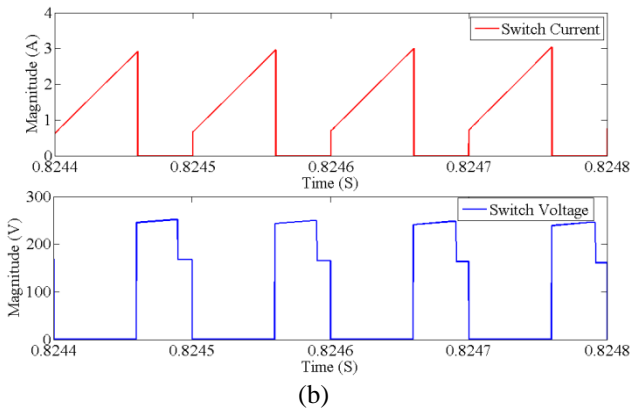

(a)

(b)
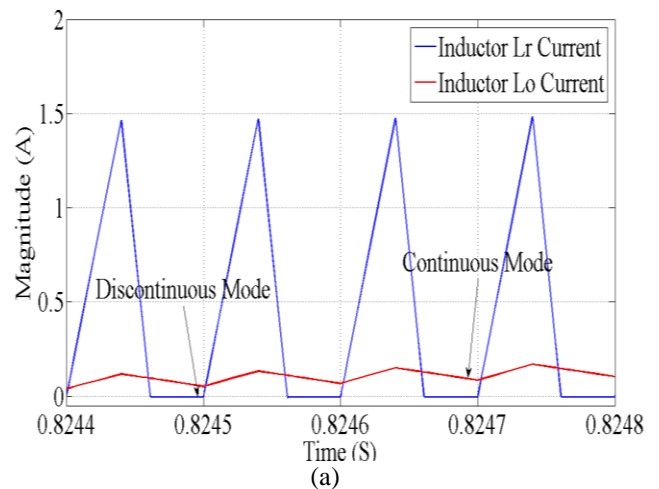
Fig. 9: Simulated waveforms of the proposed converter in steady-state (a) inductor currents; (b) switch current (i_{sw}) and voltage (V_{sw})
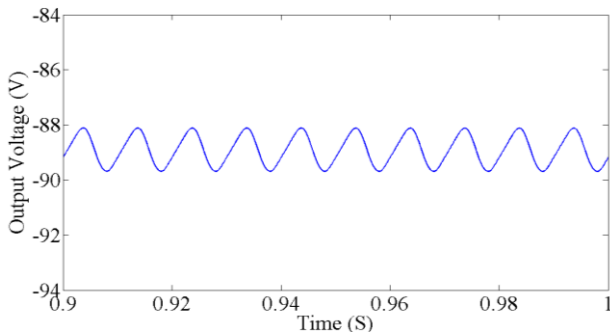

Fig. 10: Output voltage at 60% duty ratio

Figure 10 demonstrates the inverted output voltage at 60% duty ratio. The average dc voltage is about 82V with an approximate peak to peak ripple of 1.3 V (1.6%). So the proposed converter produces tightly regulated outputs for all duty ratios.
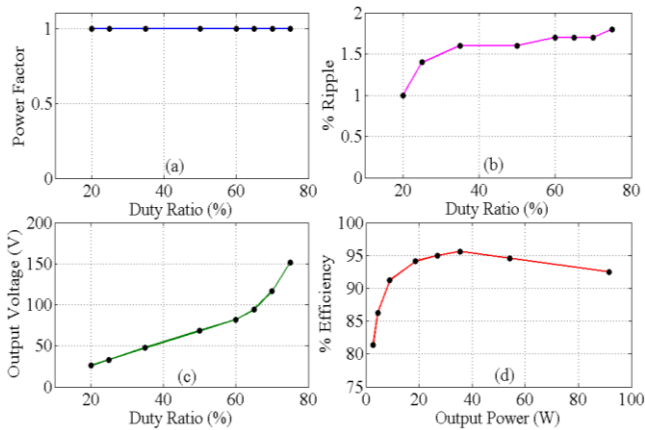

Fig. 11: Performance of the converter for different duty ratios (d_1)

Figure 11 represents the performance of the proposed converter with various duty ratios for the constant input voltage and the given load. The input power factor is unity with very less output % ripple for all the duty ratios. The simulation efficiency ranges from 82% to 95.6%. The output voltage curve represents same as voltage conversion ratio.

Figure 12 represents the performance of the proposed converter under universal voltage range ($V_s = 90$-265 V_{rms}). Throughout this range the proposed converter has exhibited good efficiencies with tightly regulated outputs having less % ripple. The power factor is also unity for both the duty ratios. These results confirm the non-isolated IB^3 converter is one of the better solutions for universal voltage range applications.
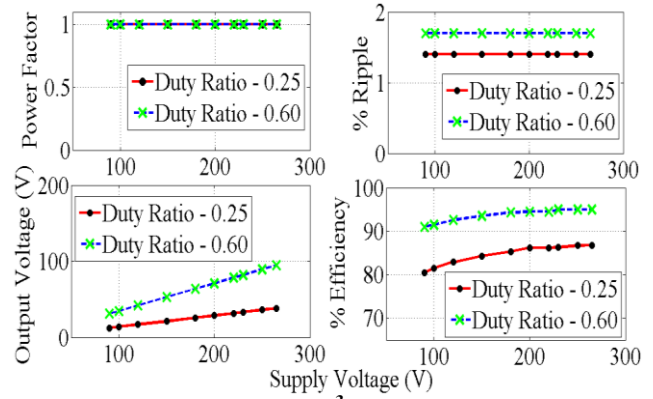

Fig. 12: Performance of IB^3 converter for universal voltages

Figure 13 shows the performance of IB^3 converter with load variation with constant supply voltage. These results showed the good performance exhibiting unity power factor, high efficiencies with less ripple factor.
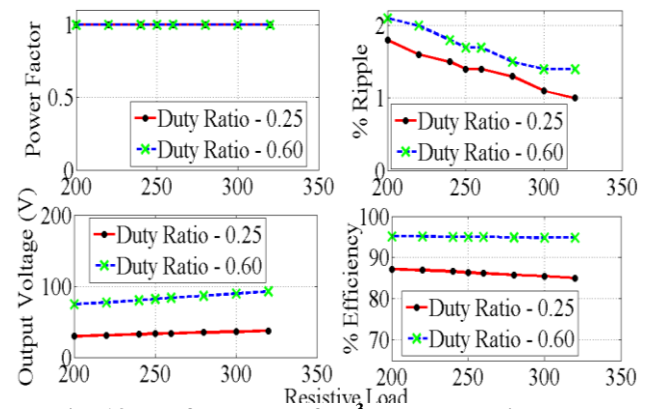

Fig. 13: Performance of IB^3 converter with load variations

VI. CONCLUSION

In this paper, an integrated non-isolated buck-boost buck (IB^3) AC-DC converter is proposed with an extended voltage conversion ratio and for unity input power factor. The proposed converter has good PFC capabilities under all the different conditions. The detailed operation and modeling of proposed converter are discussed. Necessary equations have been derived to design the converter. The features of IB^3 converter are tightly regulated dc voltage, extensive voltage gain, unity input power factor, low voltage stresses and high efficiencies. To validate the theoretical analysis the proposed converter is designed in MATLAB/SIMULINK software. The results proved that the line current %THD is very less for all conditions and satisfied the international standards (IEC 61000-3-2). Unity input power factor (UPF) at fundamental frequency is achieved for all operating conditions along with well regulated output voltages. The proposed converter is also tested for universal input voltage ranges (90–265 V_{rms}) and load variations. These results confirm that the proposed converter has better efficiencies and low output voltage ripple throughout the range. With extended voltage conversion ratio, unity power factor, higher efficiencies, the proposed converter well suits for class-C&D applications.

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NOMENCLATURE

i_{D1}, i_{D2}, i_{DF}	Diode currents
i_{Lr}	Input inductor current
i_{Lrp}	Peak value of input inductor current
i_{L0}	Output inductor current
i_{L0p}	Peak value of output inductor current
V_{Cr}	Intermediate storage capacitor Voltage
ΔV_{Cr}	Intermediate capacitor Ripple Voltage
V_{SW}, i_{SW}	Switch Voltage and Current
v_s, i_s	Supply Voltage and Current

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