International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-2 Issue-2, May 2013

Router Design Using Cadence Encounter

P. Kaveri, G.R.K. Prasad, Fazal Noorbasha

***Abstract*— As the technology is going on increasing rapidly the electronic component units are also increasing. The initial innovation for the technology growth is the internet communications and also the rapid growth in the chip density slashed the power limits. As there is no advancement in the power storage devices like batteries .so there is a need for the low power design. In all of this innovations router plays a major role in diverting the information from one to many channels , now a days it became the essential thing The concept of reconfigurable router to contribute to the creation of the next-generation energy-efficient Internet infrastructure. Through enhancement of the router architectural design, it is expected to reduce average power consumption during network operation. Depending on the traffic there is feasibility for adjusting the frequency. This project has been done in the cadence 90nm technology. System verilog for verification has been done using Synopsys tools**

Index Terms*—Low power, Routing, power *or phrases in alphabetical order, separated by commas.

I. INTRODUCTION

The tremendous success of the Internet makes it a ubiquitous infrastructure nowadays comprising an enormous number of hardware components to deliver a variety of services to end users. In the most recent years, with the aim of building a more sustainable society, research efforts have been made to look into the feasibility and benefits of applying energy-efficient techniques in information and communication technology (ICT) systems. Network-on-chip (NoC) designs are based on a compromise among latency, power dissipation, or energy, and the balance is usually defined at design time. However, setting all parameters, such as buffer size, at design time can cause either excessive power dissipation (originated by router under utilization), or a higher latency. The situation worsens whenever the application changes its communication pattern, e.g., a portable phone downloads a new service. Large buffer sizes can ensure performance during the execution of different applications, but unfortunately, these same buffers are mainly responsible for the router total power dissipation.

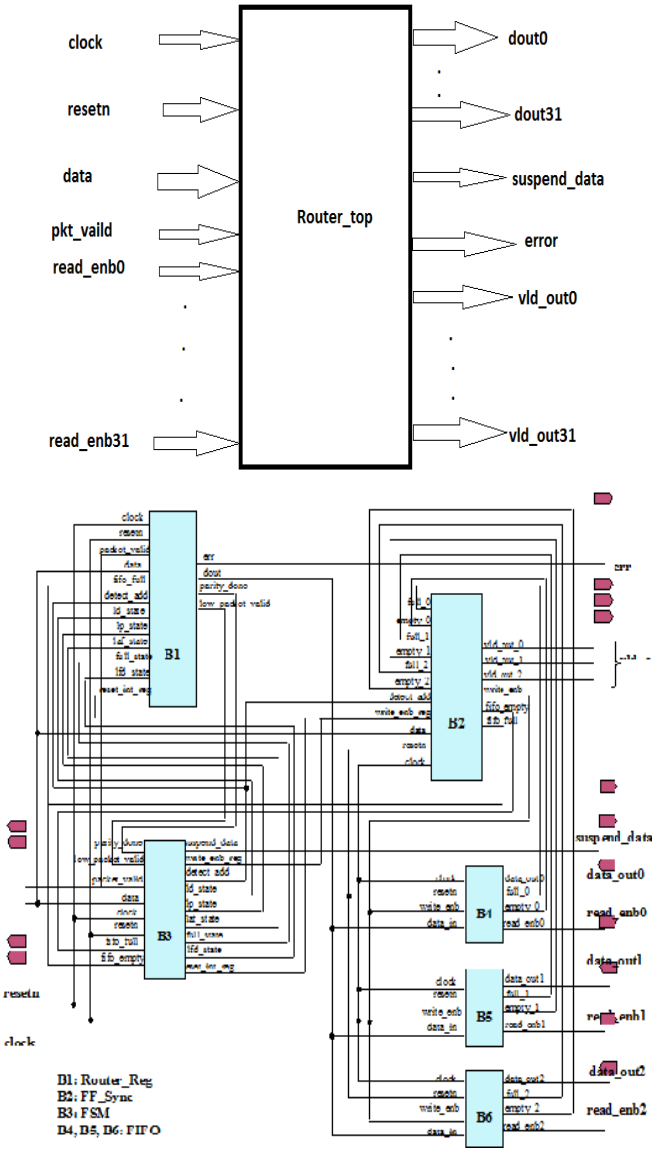
Revised Manuscript Received on 30 May 2013.
* Correspondence Author
P. Kaveri, Student of VLSI Systems Research Group, Department of Electronics and Communication Engineering, K.L University, Guntur, AP – India
G.R.K. Prasad, Asst. Professor, VLSI Systems Research Group, Department of Electronics and Communication Engineering, K.L University, Guntur, AP – India
Fazal Noorbasha, Assoc. Professor VLSI Systems Research Group, Department of Electronics and Communication Engineering, K.L University, Guntur, AP – India

Another aspect is that by sizing buffers for the worst case latency incurs extra dissipation for the mean case, which is much more frequent. In this paper we propose the use of a reconfigurable router, where the buffer slots are dynamically allocated to increase router efficiency in an NoC, even under rather different communication loads.

In the proposed architecture, the depth of each buffer word used in the input channels of the routers can be reconfigured at run time. The reconfigurable router allows up to 52% power savings, while maintaining the same performance as that of a homogeneous router, but using a 64% smaller buffer size. An optical communications repeater is a piece of equipment that receives an optical signal, converts that signal into an electrical one, regenerates it, and then retransmits it as an optical signal. In contrast, optical amplifiers, which amplify the light beam directly, are often used in transcontinental and submarine communications cables, because the signal loss over such distances would be unacceptable without them.

Radio repeaters are used in radio communication services such as Commercial or Amateur Radio. A radio repeater consists of a radio receiver connected to a transmitter. The radio signal is received, amplified and retransmitted, usually on a different frequency. Higher radio frequencies are limited to line-of-sight transmission, their range is blocked by mountains and the curvature of the Earth, so repeaters are located on hills and mountains, to retransmit the signal beyond the obstruction. Radio repeaters are also used extensively in broadcasting, where they are known as broadcast relay stations. These extend the broadcast coverage area to remote communities, outside the range of the main broadcast station. A digipeater is a blend meaning "digital repeater", particularly used in amateur radio. Store and forward digipeaters generally receive a packet radio transmission and then retransmit it on the same frequency.When providing a point-to-point telecom link using radio beyond line of sight, one uses repeaters in a microwave radio relay. A reflector, often on a mountaintop, that relays such signals around an obstacle, is called a passive repeater.Network bridging describes the action taken by network equipment to allow two or more communication networks, or two or more network segments, to create an aggregate network. Bridging is distinct from routing which allows the networks to communicate independently as separate networks. A network bridge is a network device that connects more than one network segment. In the OSI model bridging acts in the first two layers, below the network layer.

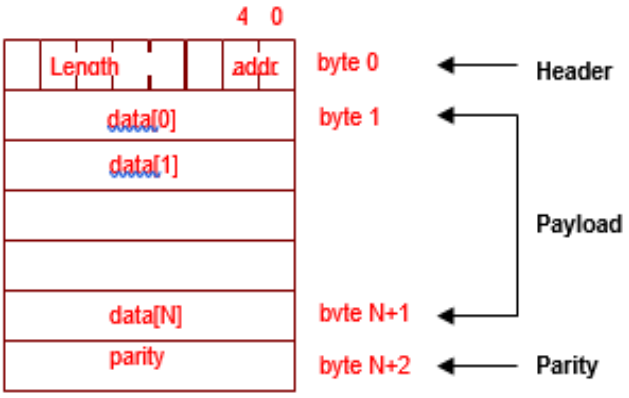
II. BLOCK DIAGRAM



Block diagram of 1*32 router

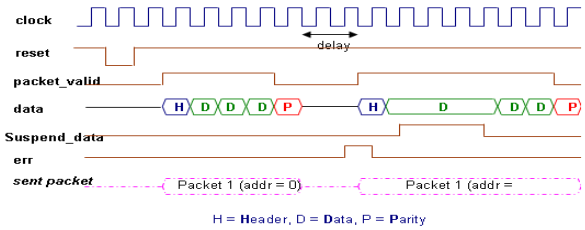
In the block diagram of the router some additional signals are used for the synchronization purpose and fifo depth must be increased to prevent the overflow of the data extra fifo will be added to prevent the loss of the data

A. *Packet format:*



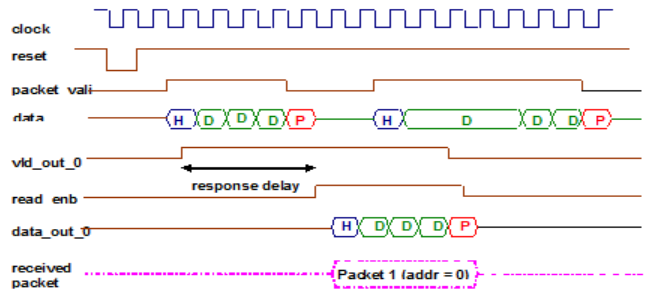
In the packet format parity bit is used to check whether the data is transferred accurately with out any error or not In byte 0 length of the data and the address will be noted.

B. *Router input protocol:*



All input signals are active high and are synchronized to the falling edge of the clock . This is because the DUV router is sensitive to the rising edge of clock . Therefore, driving input signals on the falling edge ensures adequate setup and hold time, but the signals can also be driven on the rising edge of the clock. The packet valid signal has to be asserted on the same clock as when the first byte of a packet (the header byte), is driven onto the data bus. Since the header byte contains the address, this tells the router to which output channel the packet should be routed Each subsequent byte of data should be driven on the data bus with each new rising/falling clock. After the last payload byte has been driven, on the next rising/falling clock, the packet valid signal must be disserted , and the packet parity byte should be driven. This signals packet completion. The input data bus value cannot change while the suspend data signal is active (indicating a FIFO overflow). The packet driver should not send any more bytes and should hold the value on the data bus. The width of suspend data signal assertion should not exceed 100 cycles. The err signal asserts when a packet with bad parity is detected in the router, within 1 to 10 cycles of packet completion.

C. Router output protocol:



The packet valid and the suspend data is clearly mentioned in the wave form and the introduction for the output protocol will be as similar to the input protocol.

III. FINITE STATE MACHINE

A finite-state machine (FSM) or finite-state automaton (plural: automata), or simply a state machine, is a mathematical model of computation used to design both computer programs and sequential logic circuits. It is conceived as an abstract machine that can be in one of a finite number of states.

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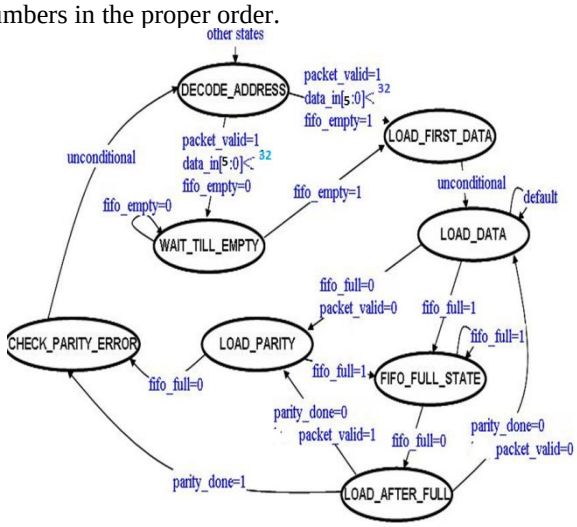
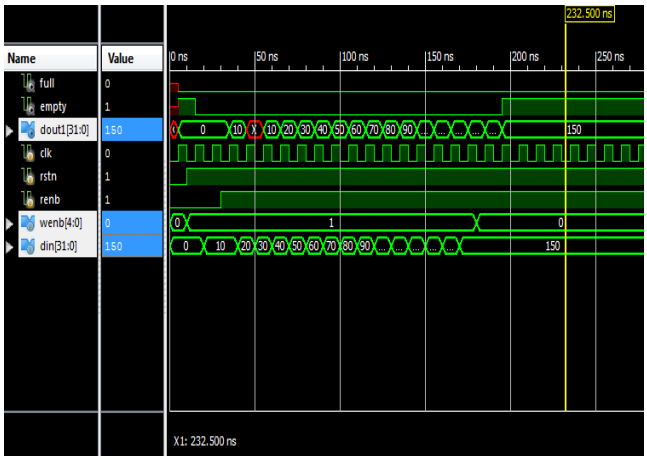
The machine is in only one state at a time; the state it is in at any given time is called the current state. It can change from one state to another when initiated by a triggering event or condition; this is called a transition. A particular FSM is defined by a list of its states, and the triggering condition for each transition. The behaviour of state machines can be observed in many devices in modern society which perform a predetermined sequence of actions depending on a sequence of events with which they are presented. Simple examples are vending machines which dispense products when the proper combination of coins are deposited, elevators which drop riders off at upper floors before going down, traffic lights which change sequence when cars are waiting, and combination locks which require the input of combination numbers in the proper order.

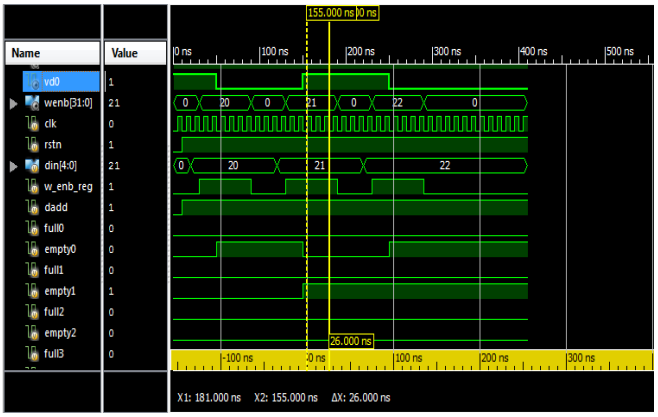


Fsm for router change of states

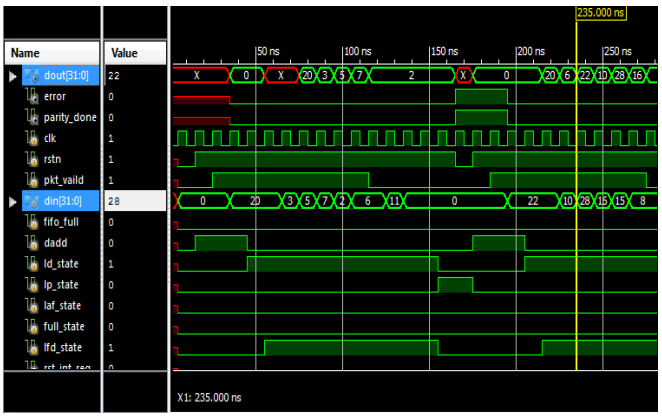
IV. RESULTS



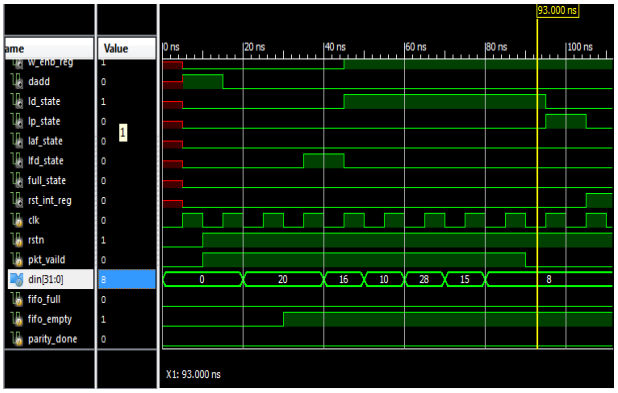
Output wave form of the FIFO



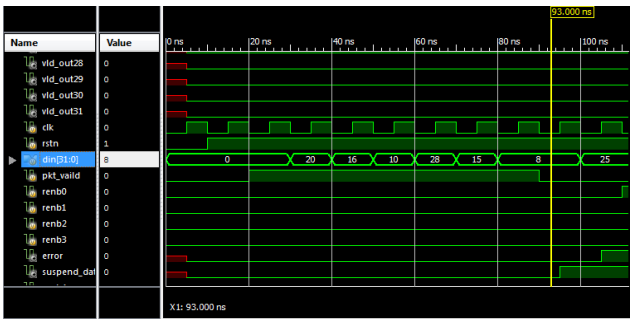
Output wave form of the synchronizer



Output wave form of the register



Output wave form of the FSM



Output showing the channel outs

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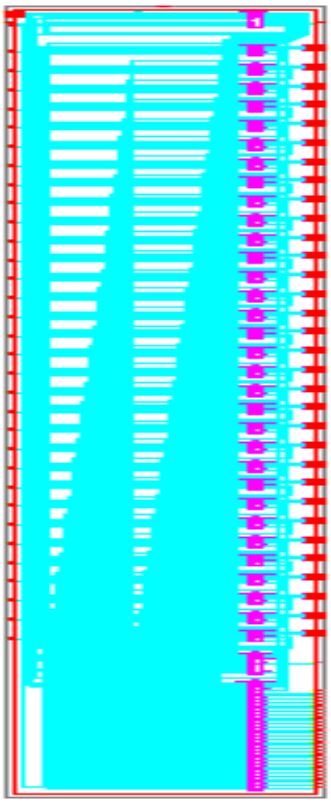


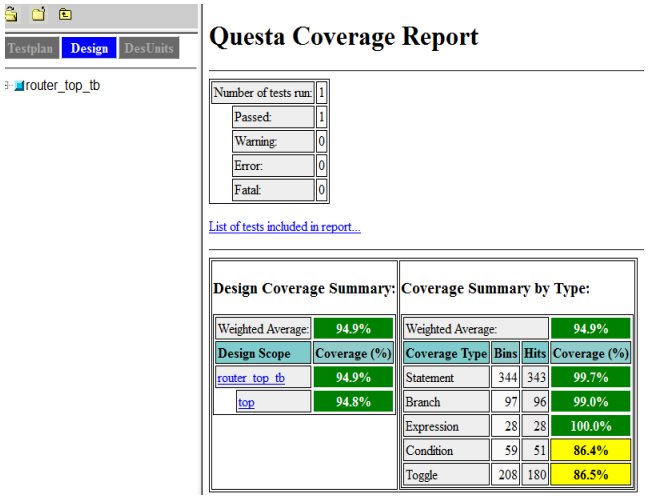
Gate level diagram of the Router

```
Incremental optimization status
================================
                        Worst  - - DRC Totals - -
                 Total    Neg       Max       Max
Operation         Area   Slack     Trans      Cap
-------------------------------------------------------------------------------
 init_delay      22823       0         0         0
 init_drc        22823       0         0         0
 init_area       22823       0         0         0

  Done mapping fifo
Warning : Instance count threshold exceeded.  Switching to manual update mode. [
GUI-12]
        : Current instance count: '2064', threshold: '2000'
        : To change the threshold set the 'gui_sv_threshold' root attribute.
  Setting attribute of root '/': 'gui_sv_update' = manual
  Synthesis succeeded.
rc:/> report power
============================================================
  Generated by:           Encounter(R) RTL Compiler v09.10-p104_1
  Generated on:           May 11 2013  03:05:06 PM
  Module:                 fifo
  Technology libraries:   slow_normal 1.0
                          slow_highvt 1.0
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

                Leakage    Dynamic     Total
Instance Cells Power(nW)  Power(nW)  Power(nW)
------------------------------------------------
fifo      2064 54565.187 411189.056 465754.243

rc:/>
```

Power report in cadence

V. CODE COVERAGE

Code Coverage is simply a measure of the code that is tested. There are a variety of coverage criteria that can be measured, but typically it is the various paths, conditions, functions, and statements within a program that makeup the total coverage. The code coverage metric is the just a percentage of tests that execute each of these coverage criteria.



Coverage report

VI. CONCLUSION

In this project, I have designed 1x32 router of 32-bit for transfer information from one network to another. The Router presented in this project reduces the power dissipation by using Clock Gating. Which in turns saves the power by only swiching one of FIFO's. The power reduces by 20% and the area reduces by 0.5%. and this router can be further integrated in to various ECU and for example in a big office network conneting various ECU's

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AUTHORS PROFILE

P.kaveri completed B.tech from Vishnu engineering college for women and pursuing masters in VLSI at KL university

G.R.K.Prasad completed masters in satyabama university , working as an Assistant professor in KL University and also persuing phd in KL University Research area includes MEMS

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Dr.Fazal Noorbasha was born on 29th April 1982. He received his, B.Sc. Degree in Electronics Sciences from BCAS College, Bapatla, Affiliated to the Acharya Nagarjuna University, Guntur, Andhra Pradesh, India, in 2003, M.Sc. Degree in Electronics Sciences from the Dr. HariSingh Gour University, Sagar, Madhya Pradesh, India, in 2006, M.Tech. Degree in VLSI Technology, from the North Maharashtra University, Jalgaon, Maharashtra, INDIA in 2008, and Ph.D. Degree in VLSI Specialization from Department Of Physics and Electronics, Dr. HariSingh Gour Central University, Sagar, Madhya Pradesh, India, in 2011. Presently he is working as a Associate Professor and Head of VLSI Systems Research Group at KL University.

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