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Coherent Circuits for Parallel Bit-Reversal

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Abstract: ***The Fast Fourier Transform is incomplete without bit-reversal. Novel parallel circuits for calculating bit reversal on data which is coming parallel are presented in this paper. The circuits are simplest, consisting of memories and multiplexers, and have the benefit of requiring the fewest multiplexers of all architectures for parallel bit reversal thus far, and tiny overall memory.***

Keywords: ***Bit Reversal, Fast Fourier Transform, Pipeline Architectures.***

I. INTRODUCTION

BIT REVERSAL is sort [1] of bit-dimension permutation [2],that permutes[3] a collection of indexed data based on the index bits being reversed. The main job of these circuits is to sort the Fast Fourier transform outputs, generally provided in the order of bit reversal.

Researchers had developed circuits that are efficient compute the bit reversal of a sequence of serial data flows [4] or parallel [5]–[11] during the last few years. Due to increasing count of high throughput FFT hardware circuits in the last several years, parallel bit reversal computing has grown in popularity. In order to have a steady stream of data coming in parallel, these designs require architectures of bit reversal with the equal parallelization. The parallel bit reversal can be implemented in a number of ways. They are determined by the sort of data storage components utilised, such as delays or memory, as well as how the bit reversal permutation is broken into additional sub- permutations. Existing research has focused on lowering the number of multiplexers or reducing the amount of memory/delays. The reduction of memory/delays, on the other hand, leads in a greater count of multiplexers, whereas the reduction of multiplexers leads in a large amount of memory being used. This paper proposes coherent circuits for parallel bit-reversal. As a result, the study investigates how to simultaneously obtain a tiny memory and a limited number of multiplexers. This is accomplished through investigating the permutation that parallel data undergoes during bit reversal, as well as the possibility of utilizing delays and memory. There are two coherent circuits for $N > P^2$ and $N <= P^2$, where N is the quantity of total data and P is the count of data coming in parallel routes in the permutation, respectively.

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In this paper we mainly focus on the circuits for $N>P^2$. These circuits use a modest amount of memory at the same time small count of multiplexers. The following is a discussion of how this paper is structured. In part II, we go through the bit-dimension permutations principles those are necessary for understanding this paper. The prior technique of parallel bit reversal is reviewed in section III. The suggested parallel circuits for bit reversal are developed in section IV. Section V compares the suggested designs to earlier techniques. Finally, the section VI, summarises the paper's principal conclusion.

II. BACKGROUND

This section summarises the key concepts in bit-dimension permutations those are necessary to comprehend the work. The reader is recommended to read [2] for a more comprehensive explanation of bit-dimension permutations.

Bit-dimension permutations applied to a collection of $N = 2^n$ data, $n \in N$, with dimensions $x_{n-1}x_{n-2}...x_0$, where $x_i \in \{0, 1\}$. A bit-dimension permutation in this context refers to the rearranging of data based on a permutation of the 'n' bits. This makes it possible to specify the permutation process on set of 'n' bits rather than 2^n values, usually several times mathematically not accessible [3]. Here $P = 2^p$ is the number of data flowing in parallel. Because the entire quantity of data is N, it is distributed in N/P cycles of clock.

In this paper σ is a function used to represent bit-dimension permutation

$$\sigma(x_{n-1}...x_m|x_{m-1}...u_0) = x'_{n-1}...x'_m|x'_{m-1}...x'_0 \quad (1)$$

It creates a new sequence $x'_{n-1}x'_{n-2...}x'_m|x'_{m-1}...x'_0$ from the vector $x_{n-1}x_{n-2}...x_m|x_{m-1...}x_0$.The leftmost n-m dimensions are parallel, whereas n-m rightmost dimensions are serial. They are separated by a vertical bar (|).

A. Elementary Bit-Exchange

A bit-dimension permutation that is simply switches 2 dimensions is known as [3]elementary bit-exchange (EBE). The single bit-exchange i.e., x_m and x_n of dimensions is represented as [4]

$$\sigma: x_m \longleftrightarrow x_n \quad (2)$$

For example, the permutation $(x_2x_1x_0) = x_1x_2x_0$ is elementary bit-exchange of dimensions x_1 and x_2.

Basically elementary bit-exchange circuits are divided into three types. Those are serial-serial (ss),i.e. two serial dimensions, parallel-parallel (pp), i.e. two parallel dimensions, and serial-parallel (sp), i.e.serial and parallel dimension.

B. Bit Reversal

A sort of bit-dimension permutation that switches the dimensions is known as bit reversal. When only serial dimensions are there, then bit reversal representation that equivalent to the permutation is

$$\sigma\,(x_{n-1}x_{n-2}\ldots x_0) = x_0\ldots x_{n-2}x_{n-1} \quad (3)$$

When parallel data is also there, then the bit reversal is given by

$$\sigma(x_{n-1}\ldots x_m|x_{m-1}\ldots x_0) = x_0\ldots x_{n-m-1}|x_{n-m}\ldots x_{n-1} \quad (4)$$

III. REVIEW OF EXISTING METHOD

The existing method [10], is based on performing basic bit-exchanges between dimensional pairs. Those are the pair's x_{n-1} and x_0, x_{n-2} and x_1, x_{n-3} and x_2, and so on. This causes the bits to be reversed in sequence, which is the core of bit reversal.

A. Theory of N > P² Bit reversal circuits:

When $N > P^2$, the bit reversal representation for the data coming in parallel is give by

$$\sigma(x_{n-1}\ldots x_{n-p}x_{n-p-1}\ldots x_m|x_{m-1}\ldots x_0) =$$

$$x_{0\ldots}x_{m-1}x_m\ldots x_{n-m-1}|x_{n-m}\ldots x_{n-1} \quad (5)$$

We can get the ss and sp permutations by splitting this permutation.

$$\sigma_1(x_{n-1}\ldots x_{n-m}x_{n-m-1}\ldots x_m|x_{m-1}\ldots x_0) =$$

$$x_{n-1}\ldots x_{n-m}\underline{x_m\ldots x_{n-m-1}}|x_{m-1}\ldots x_0 \quad (6)$$

$$\sigma_2(x_{n-1}\ldots x_{n-m}x_{n-m-1}\ldots x_m|x_{m-1}\ldots x_0) =$$

$$\underline{x_0\ldots x_{m-1}}x_{n-m-1}\ldots\underline{x_m|x_{n-m}\ldots x_{n-1}} \quad (7)$$

Where σ_1 denotes ss and σ_2 denotes sp. Here the permutations order is random i.e. = $\sigma_1 \circ \sigma_2 = \sigma_2 \circ \sigma_1$. For the sp permutation, the number of delays is

$$D_{sp} = \sum_{j=n-p}^{n-1} 2^j = \frac{2^{n-p}-2^n}{1-2} = N - (N/P) \quad (8)$$

Multiplexers required are

$$M_{sp} = \sum_{j=n-p}^{n-1} 2^p = p.P = P.\log_2 P \quad (9)$$

and latency is given by

$$Lt_{sp} = (D/P) = (N/P) - (N/P^2) \quad (10)$$

A bank of memory calculates the ss permutation σ_1.Because σ_1 has no effect on the parallel dimensions and is independent of them, all memories perform the identical permutation. The n-2p lower serial dimensions order is flipped in this permutation. As a result, the bit reversal of 2^{n-2p} serial data is the operation that each memory performs. The bit reversal is determined by retrieving data in the order of bit reversed after it has been loaded in memory in natural order. Similarly, if the data is loaded in the bit-reversing order, then bit reversal is accomplished by retrieving that data in normal order from memory. The bit reversal of input data is calculating by altering the addresses of memory between natural order and bit reversed order. The memory size is equals to

$$\text{Memory Size}_{ss} = 2^{n-2p} = (N/P^2) \quad (11)$$

Since parallel branch has one memory, the count of memories given by

$$\#Mem_{ss} = P \quad (12)$$

and for ss permutation the overall memory is

$$Mem_{ss} = Memorysize_{ss} \bullet \#Mem_{ss} = (N/P) \quad (13)$$

Because the write and read addresses are same, each memory's latency is same as its size, i.e.

$$Lt_{ss} = (N/P^2) \quad (14)$$

Finally, because permutation is accomplished simply changing the reading and writing addresses of the memories, there is no need for a multiplexer to the memories. The overall memory cost of the existing technique is calculated by adding the costs of the sp and ss permutations.

$$Mem = D_{sp} + Mem_{ss} = N \quad (15)$$

Only the sp permutation includes multiplexers, so the overall latency given by

$$Lat = Lt_{sp} + Lt_{ss} = N/P \quad (16)$$

B. B. Architecture of N>P² Bit Reversal Circuits:

Figure 1 shows the existing method of Bit reversal circuits for N=32 and P=4.The circuit consists of 8 memories and 8 multiplexers. Based on the selection line of Multiplexer the data loaded into the memories. Here the addresses for each memory are generated by the control counter. The control signals for the multiplexer are generated by the address generator.

IV. PROPOSED ARCHITECTURE

The architecture of N>p2 proposed method is shown in the figure 2.As shown in figure1 the existing method circuits for N=32 and P=4, consists of 8 memories and 8 multiplexers. Among the 8 memories, 2 memories are grouped into single memory so that there are 4 memory block as shown in the figure2.

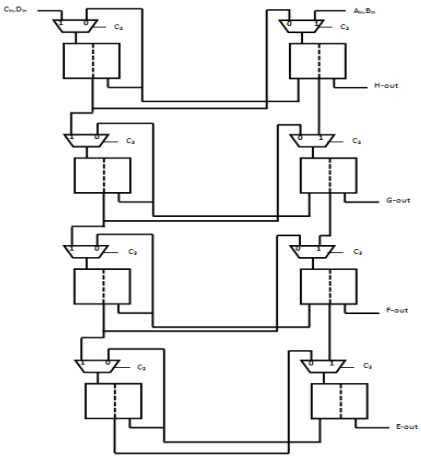

Fig1. Circuits of Bit Reversal for N=32 and P=4

This architecture uses the concept of grouping memories and multiplexing methods. Two memories are grouped together into single memory based upon the addresses of the memories. Because of that grouping of memories number of multiplexers is reduced.

Here the addresses for each memory are generated by the address generator. The address generator consists of multiplexers and control counter. The multiplexers of address generator are 1-bit, so multiplexer's area is negligible. Based on the MSB bit of control counter the address of first memory is bit reversed. The control signals for the multiplexers also depend upon the MSB bit of control counter. When the MSB bit is 1the input data is given to the memory and when MSB is 0 data from internal signals is given to the memory. Here x1_in, x2_in, x3_in, x4_in are input data signals and y1_out, y2_ out, y3_ out, y4_ out are output data signals.

Here few internal signals are used to trace the data apart from the input, output and control signals.

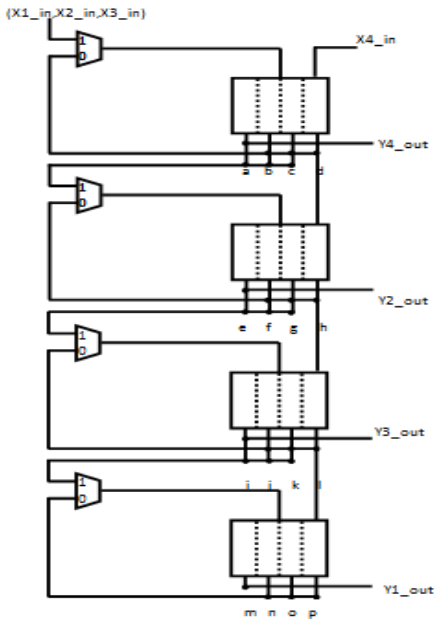

Fig2. Proposed Circuit of Bit Reversal for N=32 and P=4

In this the total memory used is

$$\text{Memory} = N$$

Number of Multiplexers used is

$$\text{Multiplexers} = (P/2)\log_2 P$$

and the overall latency of this circuit is

$$\text{Latency} = N/P.$$

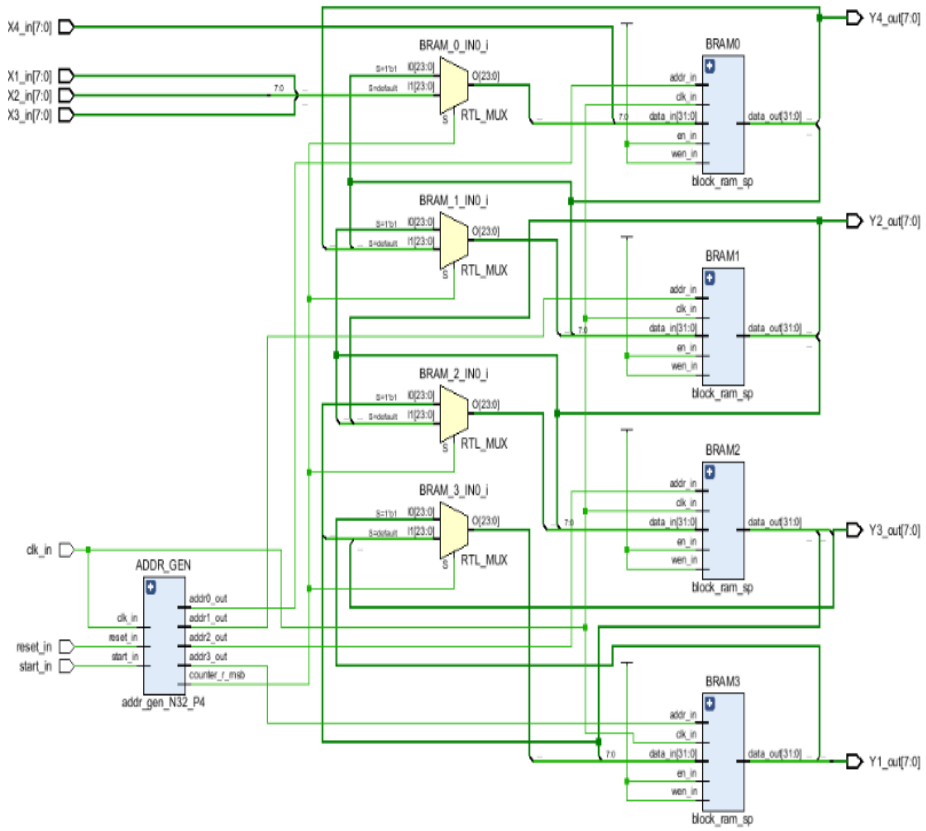

Fig3: Schematic view of Proposed Bit Reversal Circuits

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V. RESULTS

Implementation and Synthesis of both proposed and previous architectures are done using Virtex-7 XC7VX330T- 3-FFG1157 FPGA family in order to make an appropriate comparison in terms of Number of LUTs, Flip-Flops used and utilised power. Fig3 shows the schematic view of proposed architecture. In the proposed Architecture the number of multiplexers is reduced as compared to the existing method. So the number of LUTs is decreased and the power is also reduced as shown in the figure4 and figure5.Comparision between the proposed method with the existing method are tabulated in table1. Verilog HDL Coding has been used to implement the architectures.

VI. CONCLUSION

In this brief, Optimized Parallel bit reversal circuits is implemented. The suggested circuit has a low memory need and at the same time, the number of multiplexers is reduced. The counter is used to create the necessary signals for regulating multiplexers. The proposed architecture requires a memory of N addresses and $(P/2)\log_2 P$ multiplexers. This suggests a finite amount of memory as well as relatively small number of multiplexers.

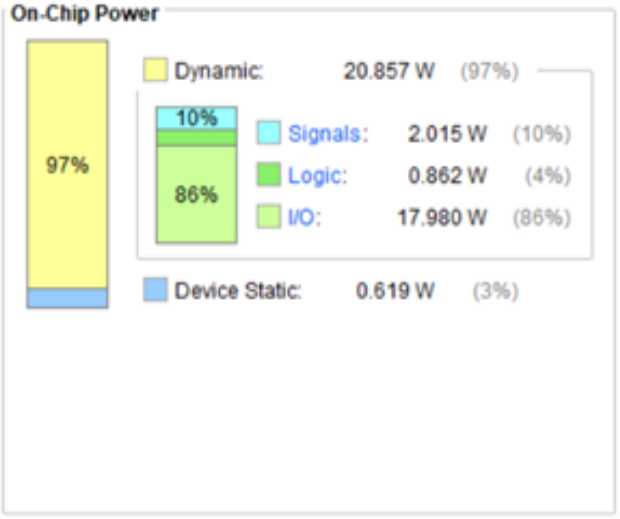

Fig4: Power report of Existing Bit Reversal Circuit

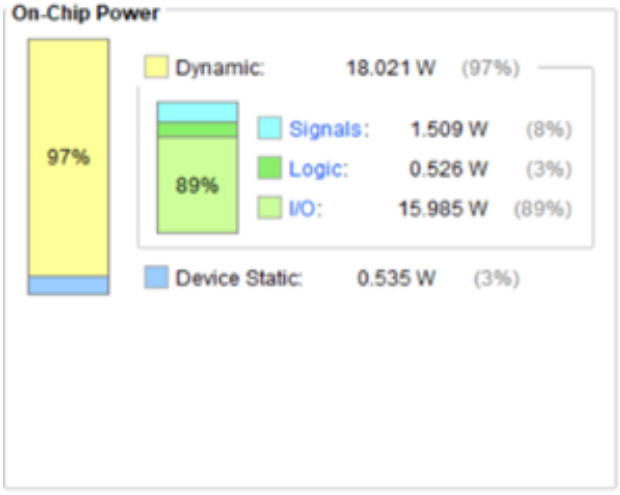

Fig5: Power Report of Proposed Bit Reversal Circuits

Table I: Comparison of Existing Bit reversal circuits with the Proposed Bit reversal circuits.

Architecture	LUT	FF Used	POWER (W)	FREQUENCY (MHz)
Existing	259	5	21.476	298
Proposed	227	5	18.556	298

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